

Optimizing the High-Electron-Mobility Transistor Amplifier Performance

Lukas Lang

ETH Zürich, D-CHAB

langl@student.ethz.ch

April 19, 2017

Abstract

In order to improve the output signal-to-noise ratio of the typical measurement schema used in superconducting circuit based experiments, I determined the performance of the high-electron-mobility transistor (HEMT) amplifiers as a function of bias voltages in three different types of measurements. I measured the amplified transmission through a HEMT using a vector network analyzer, a Virtex 6 field-programmable gate array, as well as a power spectrometer. The performance of the amplifier as a function of its bias voltages was then characterized by the absolute transmission in the case of the first experiment, and the gain and noise temperature in the case of the other two, respectively. I demonstrated improvement of the amplifier performance using this technique compared to the standard use of the specified voltages given by the manufacturer by an increase of 5-7 dB gain and a factor of 2 in noise temperature. I postulate with evidence that this is due to the loss of current in the DC cabling between the voltage source and amplifier. Finally, I constructed a new DC breakout box for Aphrodite; the new cryogenic fridge.

Supervised by

Theodore Walter

and

Philipp Kurpiers

Supervising professor: Prof. Dr. Andreas Wallraff

Contents

1	Introduction & Motivation	1
2	Theory	1
3	Experimental methods	3
3.1	VNA measurements	3
3.2	FPGA measurements	5
3.2.1	Absolute gain and noise estimates	8
3.3	Power specturm measurements	9
4	Results & Discussion	11
4.1	Voltage decay	11
5	Summary	12
6	Acknowledgements	13
7	Bibliography	13
8	Appendix	14
A	Voltage settings	14
B	DC Cabling	15
B.1	Breakout box	15
B.1.1	Cabeling	15
B.1.2	Assembly	18
B.1.3	Checks	18
B.2	DC cabeling	18
B.2.1	Interconnections	19

1 Introduction & Motivation

The goal of this project was to determine the performance of the high-electron-mobility transistor (HEMT) amplifiers used as the initial amplifier in the typical measurement schema employed in superconducting circuit based experiments, and to find their optimal bias voltages. Here the performance of an amplifier refers to its capability to amplify the signal while introducing a comparatively low amount of noise. This is an essential feature of the first amplifier in a circuit in order to achieve a high signal-to-noise ratio (SNR) at the output (see section 2).

Bias voltages are applied between the gate or drain and the ground of the HEMT and determine its transmission characteristics. I therefore swept these two control parameters to determine the settings for the best HEMT performance. I employed several parameters to quantify the HEMT performance in the three series of measurements performed. In the first experiment, the absolute transmission $|S_{21}|$ of the circuit was used as an indicator. In the second experiment, the peak and mean power of the output power spectrum in relative units were used to estimate the signal and noise power, respectively. For the final experiment, the absolute gain was measured.

Between the second and third series of measurements, I soldered the DC cabling for the newly built cryostat (Aphrodite) (see section B on page 15), as it was planned to do the third experiment there once finished. The cabling is used to set the DC voltages/currents for the various HEMT amplifiers and coils inside the cryostat.

In the following, an introduction to the theory of SNR propagation in circuits will be given, followed by an overview of the conducted experiments. Afterwards, the most important results are discussed.

2 Theory

To show how the SNR is affected by different components of a circuit, I employed the following model for signal and noise propagation.

The contribution to noise of each component is assumed to follow the power spectral density (PSD) of thermal noise, given by

$$S(\omega, T) = \frac{\hbar\omega}{e^{\frac{\hbar\omega}{k_B T}} - 1} \quad [1]. \quad (2.1)$$

Given the signal $s_{\text{in}}(\omega)$ and noise $n_{\text{in}}(\omega)$ at the input of a component, its output is given by $s_{\text{out}}(\omega)$ and $n_{\text{out}}(\omega)$. The relations for the case of an attenuator are [2] (attenuation $0 \leq A \leq 1$, temperature T_A)

$$s_{\text{out}}(\omega) = A \cdot s_{\text{in}}(\omega) \quad (2.2)$$

$$n_{\text{out}}(\omega) = A \cdot n_{\text{in}}(\omega) + (1 - A) \cdot n_{T_A}(\omega), \quad (2.3)$$

whereas they are given by

$$s_{\text{out}}(\omega) = G \cdot s_{\text{in}}(\omega) \quad (2.4)$$

$$n_{\text{out}}(\omega) = G \cdot (n_{\text{in}}(\omega) + n_{T_N}(\omega)) \quad (2.5)$$

for amplifiers (gain $G \geq 1$, noise temperature T_N).

The noise added by an amplifier can be attributed to a noise temperature T_N (independent of the real temperature) as a figure of merit (Eq. (2.5)). To quantify the impact on the signal and noise of a component/circuit, the noise factor

$$F := \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \quad (2.6)$$

is introduced.

Given an exemplary circuit with an amplifier, followed by an attenuator, the noise factor F is given by

$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} = \frac{s_{\text{in}}}{n_{\text{in}}} \cdot \frac{n_{\text{out}}}{s_{\text{out}}} \quad (2.7)$$

$$= \frac{s_{\text{in}}}{n_{\text{in}}} \cdot \frac{(n_{\text{in}} + n_{T_N}) \cdot G \cdot A + (1 - A)n_{T_A}}{G \cdot A \cdot s_{\text{in}}} \quad (2.8)$$

$$= 1 + \frac{n_{T_N}}{n_{\text{in}}} + \frac{(1 - A) n_{T_A}}{G \cdot A n_{\text{in}}}. \quad (2.9)$$

This result is a special case of Friis formula for noise [3]. For $\frac{1-A}{G \cdot A} \ll 1$ (given for an amplifier with high gain), the noise introduced by the attenuator can be neglected. In Fig. 1, the output SNR and the inverse noise factor F^{-1} are shown for $G = 20, 30$ dB (blue and green respectively) and $A = -10$ dB. Although the total noise at the output is higher for the high-gain (green) circuit, the output SNR is greater, making it the better measurement chain. This is what makes the noise factor, or respectively its inverse, a suitable metric for the performance of a measurement chain compared to the total gain or noise temperature alone. Determining F for the general case of multiple components shows that noise sources after the first amplifier are negligible when the amplifier is good enough.

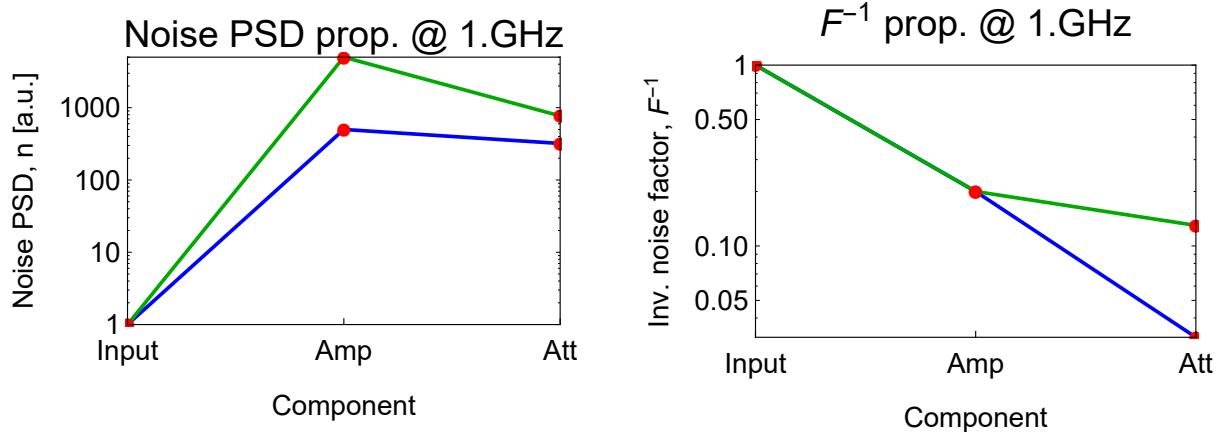


FIG. 1: The total noise and F^{-1} for a circuit consisting of an amplifier (20 dB, blue and 30 dB gain, green) and an attenuator (-10 dB). The points show the values directly after each component. F^{-1} (and therefore the output SNR) is a lot higher for the circuit with the stronger amplifier, even though the absolute noise power is larger.

3 Experimental methods

3.1 VNA measurements

In the first experiment, I measured the transmission parameter $|S_{21}|$ as a function of frequency using a vector network analyzer (VNA, Agilent N5230C). The circuit under investigation is shown in Fig. 2, in which the VNA was connected to the input and output of the circuit. As the schematic shows, the circuit was cooled to temperatures in the range 0.01–2.8 K (achieved inside the cryostat), with the HEMT (LNF-LNC4.8A s/n 205) at 2.8 K. The circuit also contained three attenuators (XMA-2082-6243-20 cryogenic attenuators, XMA Corporation) before the amplifier used to thermalize the input cable, four circulators (RADC-4-8-Cryo-0.02-4K-S23-1WR-b, Raditek 4-8) and a bandpass filter (Keenlion KBF 4/10 2S, Keenlion Microwave Technology Co., Ltd.). The circuit was coupled to a resonator containing a qubit. Due to the narrow bandwidth of the resonator, this could be expected to influence the measurements only in a very small range of frequencies. To find the optimal settings, I varied the bias voltages, starting from the values specified by the manufacturer, $(V_{\text{Drain}}, V_{\text{Gate}}) = (500 \text{ mV}, 320 \text{ mV})$. First, I investigated the immediate vicinity of these voltages, I then increased voltages until the transmission started to decline again. Having found the maximum at $(720 \text{ mV}, 560 \text{ mV})$, I varied the voltages around this point to investigate the nature of this optimum. A list of investigated voltage settings can be found in Table I on page 14. A total of 39 voltage settings were measured. For each of those, $|S_{21}|$ was measured as a function of frequency, with 10 000 points between 3–14 GHz. The raw data for all points are shown in Fig. 3:

The transmission is higher in the region between 4–8 GHz, which is expected due to the bandpass filter and the HEMT. At 6.96 GHz, there is a sharp dip in the transmission

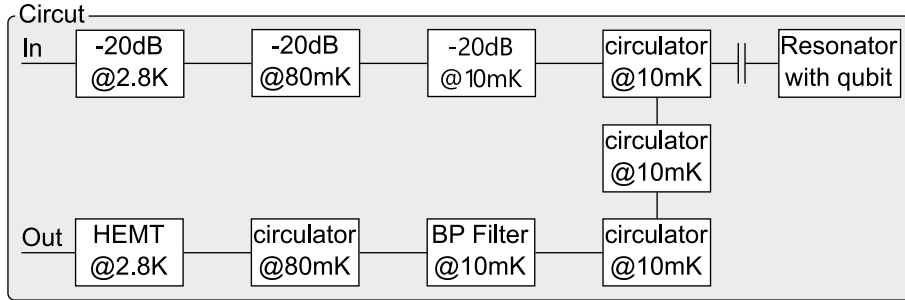


FIG. 2: The circuit used for the VNA and field-programmable gate array (FPGA) measurements. Left to right corresponds to outermost (warmest) chamber of the cryostat to innermost (coldest) chamber. The circuit is weakly coupled to a resonator with a qubit at the base.

due to the previously discussed resonator. Also, transmission decreases slightly towards higher frequencies, which is most likely caused by the frequency dependent loss of the cables (see later for a detailed discussion). The dip in transmission around 4.2–4.7 GHz could not be attributed to any component in the circuit.

As these features are found for every measurement setting, they do not influence the result of the performance measurements, since only relative performance matters.

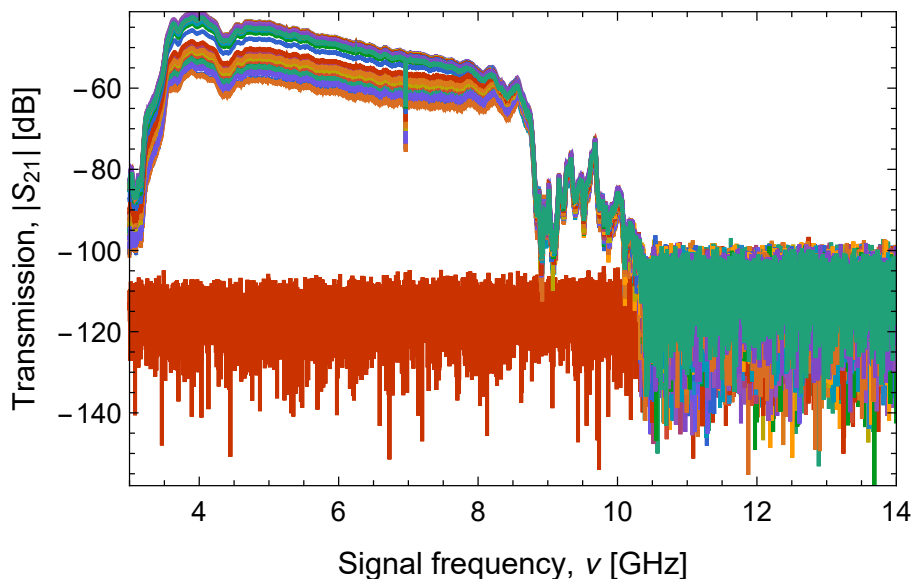


FIG. 3: The raw data recorded for all voltage settings investigated.

The flat red trace in Fig. 3 was recorded with both voltages set to 0 mV. The transmission being nearly 0 implies that the attenuation is too high to be measured, and that the amplifier does not behave as a through with no impact on the signal amplitude. It is therefore not possible to turn the amplifier off in order to get a reference measurement. As it was not possible to open the cryo and access the cabling, no reference line or bypass switch could be added. For this reason, only the transmission of the complete circuit was available.

For all further evaluations, I divided the frequency range into 250 MHz blocks which were averaged. The largest transmission of the amplifier was achieved with bias voltages above the specified ones, as seen by the orange circle in the contour plot of Fig. 4, which shows the results for the 4.5–4.75 GHz range. To check whether this observation is true for the whole frequency range, the traces of the three points marked in Fig. 4 are compared in Fig. 5. The traces correspond to the specified settings (red & dot-dashed, $(V_{\text{Drain}}, V_{\text{Gate}}) = (500 \text{ mV}, 320 \text{ mV})$), the settings which achieved optimal transmission (yellow & solid), and those with highest peak/mean power (blue & dashed, see section 3.2 for more details). For all future comparisons, the same three settings were used. The traces being nearly parallel suggests that the relative performance is not affected by the various features of the curves described above.

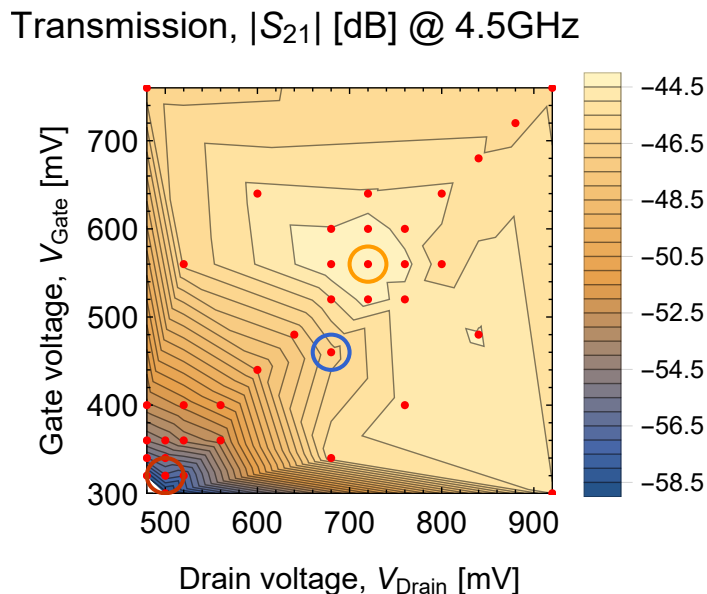


FIG. 4: Measured $|S_{21}|$ at 4.5 GHz for every voltage setting investigated. The red dots show the measurements, the colors in-between show estimates based on a linear interpolation. For the three voltage settings marked, the frequency dependent transmission can be found in Fig. 5.

3.2 FPGA measurements

The goal of the second experiment was to reproduce the results of the first by measuring the output power spectrum instead of the absolute transmission, as well as to acquire data about the noise performance for further insights into the behavior of the HEMT. I performed the measurements with the same circuit as in the first experiment (Fig. 2). In this case, I measured the power spectrum using an FPGA (field programmable gate array, Virtex-6, Xilinx) by applying a coherent signal to the circuit. After exiting the circuit it passes through a down conversion board (BluFors 1 down conversion board). Down conversion is achieved by mixing with a local oscillator using a 4-way mixer (one

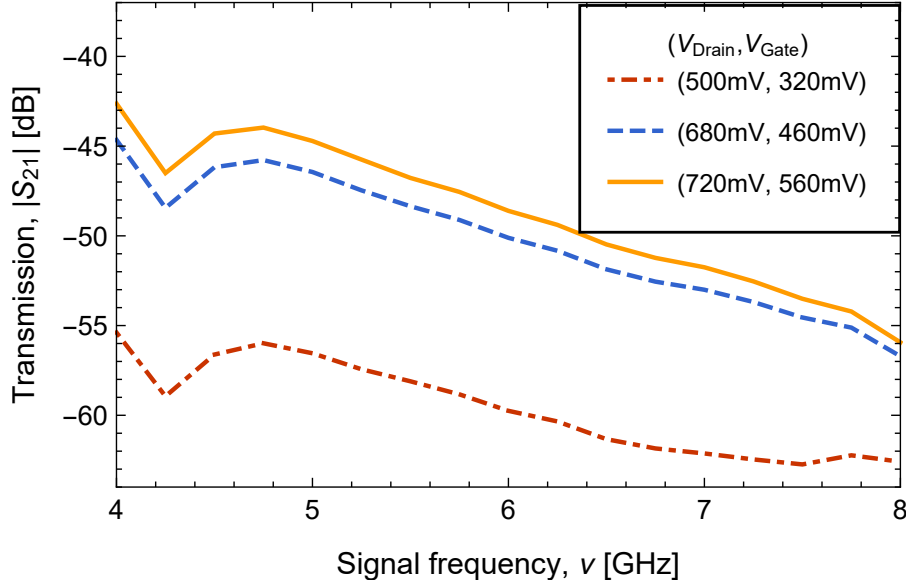


FIG. 5: The absolute transmission parameter $|S_{21}|$ as function of frequency for the three voltage settings marked in Fig. 4. There is more than a 10 dB increase in transmission between the specified settings and the optimal ones.

output terminated). The output quadrature signal from the mixer is filtered (lowpass filter) and amplified, and routed to the ADC (analog to digital converter) of the FPGA which performs a time resolved measurement of the voltage.

For every bias voltage setting, I swept the signal frequency between 4–8 GHz in 250 MHz steps and recorded the signal power for 8192 points spaced 1 ns apart. A discrete Fourier transform of this data reveals the power spectral density which is 1 GHz wide (signals of larger detuning are folded back into this region) and has a resolution of ~ 122 KHz.

To verify results, I chose the same bias voltage settings as for the first experiment (Table I on page 14), in addition to which I investigated the region with the largest $|S_{21}|$ parameter with a smaller step size (settings in Table II on page 14).

I also performed a reference measurement where the cryostat was excluded from the circuit by replacing it with a through.

The output power spectra each show a narrow signal peak, as well as some much lower peaks at other frequencies which are most likely LO leakage and some backfolded signals, as shown in Fig. 6. For each of the 78 measurements, I extracted two parameters from the power spectrum: The peak power P_p , defined as the highest value in the power spectrum and the mean power P_m , defined as the average of all points in a 10 MHz band around 0 MHz (excluding the signal peak).

While these parameters are not absolute gain and noise measurements, they provide estimates for both, which can be used to compare different bias voltages. P_p can be used as an estimator for gain, evidenced by the behavior being qualitatively the same as for $|S_{21}|$ (first experiment, Fig. 4). P_m is an estimator for noise and shows a different behavior,

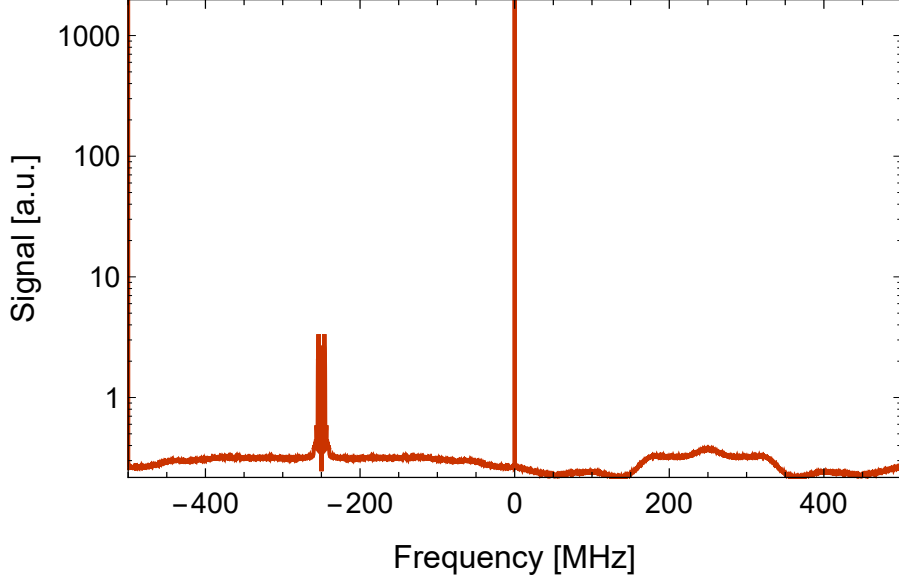
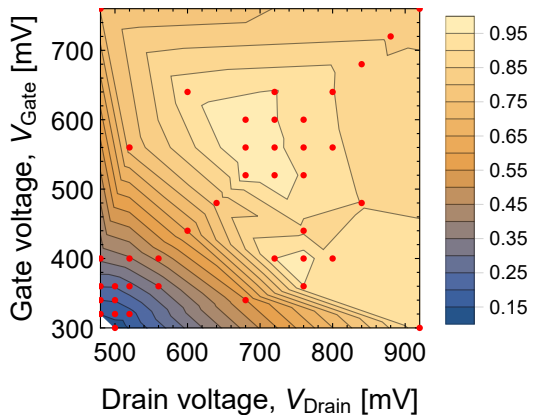


FIG. 6: An exemplary power spectrum that was measured during the FPGA measurements. The signal is the peak at 0 MHz, the features to the left and right are most likely LO leakage and some backfolded signal respectively.

where it is mostly flat for lower voltages with a sudden increase when the voltages are increased above a certain threshold. Both parameters are shown in Fig. 7 for an input frequency of 4.5 GHz.

a) Peak power, P_p [a.u.] @ 4.5GHz



b) Mean power, P_m [a.u.] @ 4.5GHz

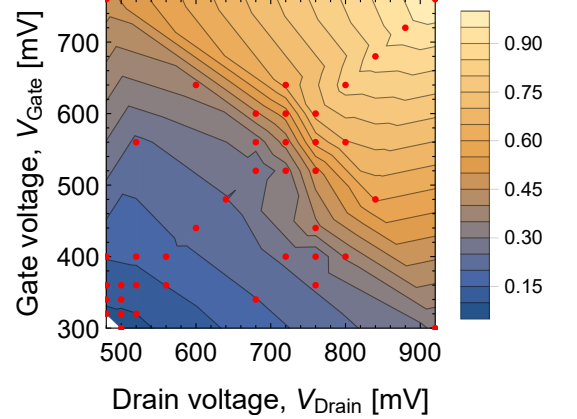


FIG. 7: The normalized peak (a) and mean power (b) at 4.5 GHz for the complete measurement range. The red points show the measurements, the colors between the points come from linear interpolation.

Dividing P_p by P_m gives an estimate for the SNR (since the signal P_p is several orders of magnitude higher than P_m , P_m is not subtracted from P_p to get the signal contribution). As the mean power increases drastically above a certain threshold, the SNR gets lower again for high bias voltages (see Fig. 8 for the case of 4.5 GHz input frequency), contrary to what the peak power alone suggests. Again, the three settings are compared as functions of frequency, where the second point (blue, dashed) was chosen to be the point of highest

overall P_p/P_m . This comparison shows that the optimal point in terms of transmission is already beyond the maximal SNR (Fig. 9).

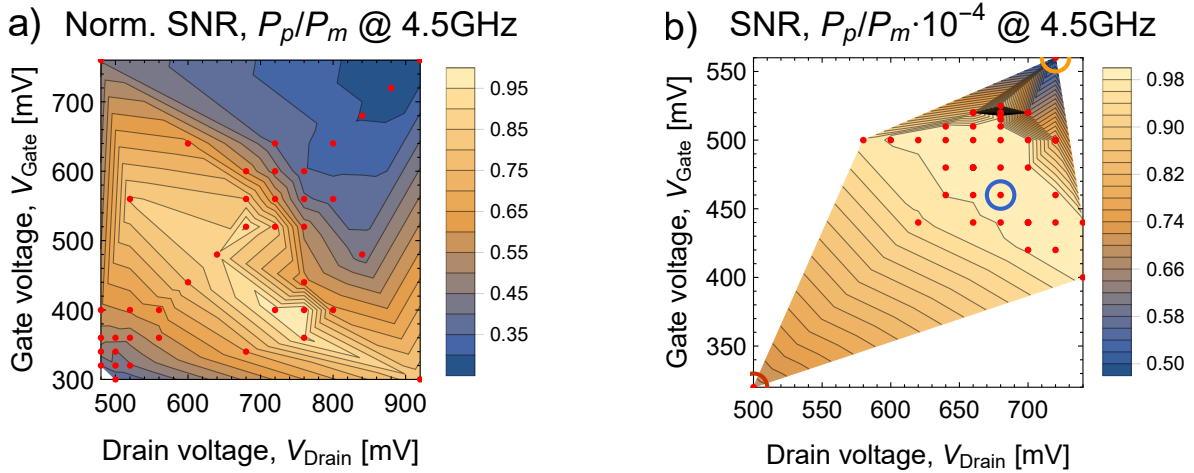


FIG. 8: The peak over mean power $\frac{P_p}{P_m}$ at 4.5 GHz for the complete measurement range (a) and zoomed in on the plateau region (b). The red points show the measurements, the colors between the points come from linear interpolation.

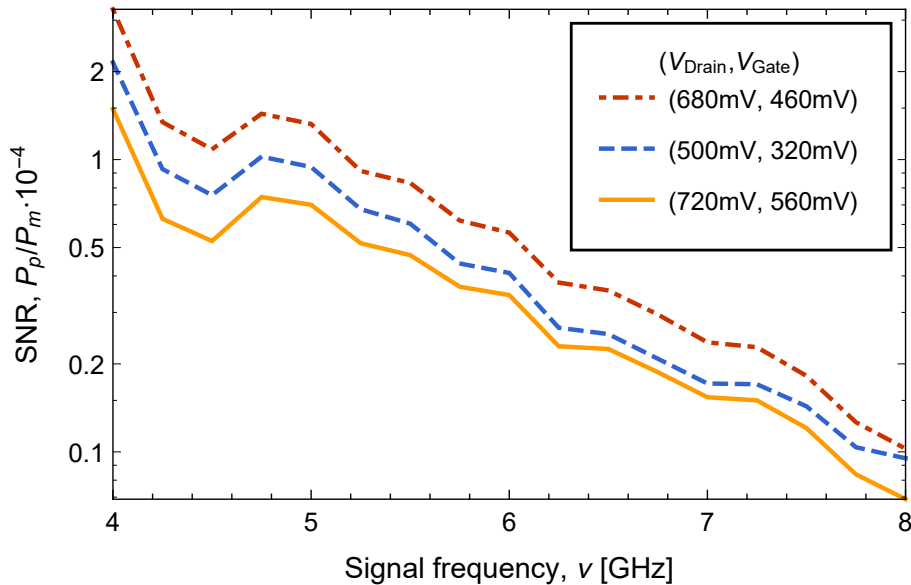


FIG. 9: Peak over mean power $\frac{P_p}{P_m}$ as a function of frequency for the three voltage settings chosen.

The relative performance between the different settings is neither influenced by the slope of P_p/P_m , nor by any of the other artifacts (such as the drop around 4.5 GHz) present.

3.2.1 Absolute gain and noise estimates

I attempted to extract values for the absolute gain and noise temperature from the available FPGA measurement data.

The y -axis of the power spectrum was calibrated using the spectrum with the cryo excluded. Since the input power is known and the y -axis is proportional to the output power, the spectrum can be scaled accordingly and any remaining difference can be attributed to the circuit inside the cryostat.

To simulate the circuit, the signal and noise propagation equations from section 2 on page 1 were applied to the list of components inside the cryo. For the cables, frequency dependent losses from measurements previously performed by P. Kurpiers were used, for the remaining components (excluding the HEMT), constant attenuations were assumed. The parameters G and T_N of the HEMT were introduced as variables. Knowing both the signal P_p and the noise power P_m of the complete circuit, G and T_N could be determined. The results for the HEMT parameters show that both absolute gain and noise temperature have been improved consistently over the whole frequency range by changing the bias voltages (Fig. 10). The feature around 4.5 GHz is the same as in the other results, and is most likely not due to the HEMT. The steady increase in noise temperature does not necessarily originate from the HEMT, it could also be due to some frequency dependent loss of another component that has not been considered in this estimate. Since one of the outputs of the 4-way mixer is terminated, the noise temperature is two times larger than it would be if both outputs had been recorded and combined appropriately.

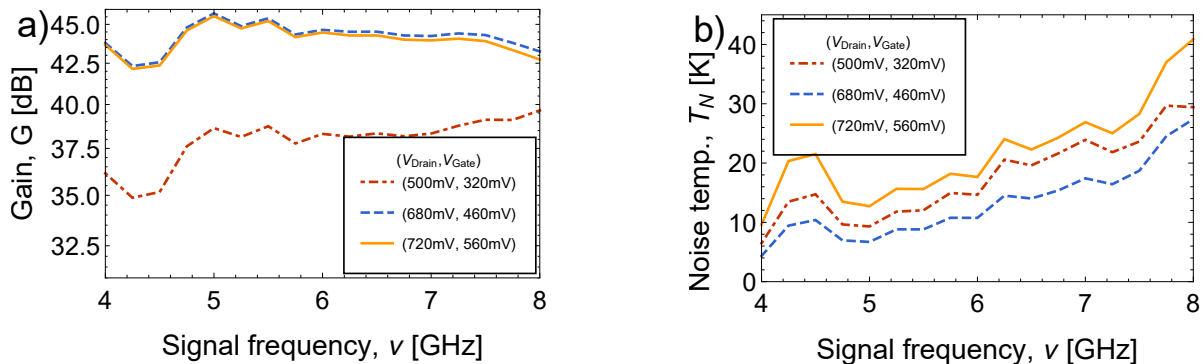


FIG. 10: The absolute gain (a) and noise temperature (b) determined for the HEMT in the circuit shown in Fig. 2 on page 4 using the method described in section 3.2.1. Both the gain and the noise temperature have been improved compared to the specified settings.

3.3 Power spectrum measurements

Since neither of the two experiments described were able to directly measure gain and noise temperature, I performed a third experiment on another circuit. As the cabling of the cryostat used in this experiment (Aphrodite) could be accessed, a reference line was added which allowed measuring the absolute gain. The measurement line and the reference line are both shown in Fig. 11. The two lines differ only by the HEMT in terms of components and cable lengths. However, the lines have not been compared explicitly (as could be done by removing the HEMT from the measurement line). Due

to time constraints, the measurements were performed at room temperature, where the optimal bias voltages could not be reached. For this reason, no noise temperatures were determined.

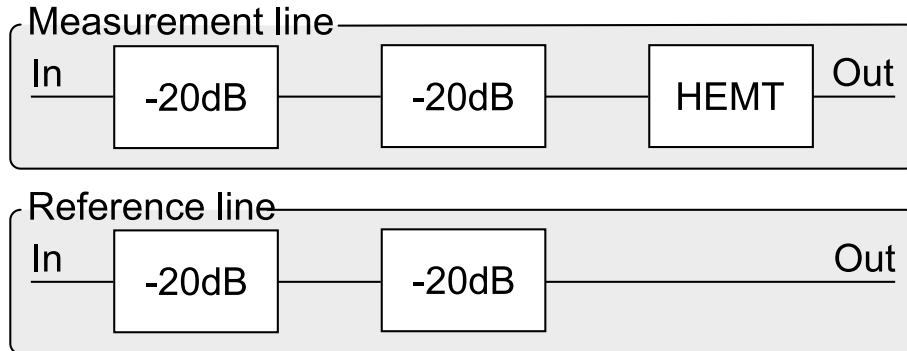


FIG. 11: The circuit use to perform the third experiment, where the absolute gain was determined. The reference line is identical to the measurement line except for the HEMT.

Initial settings were again the specified bias voltages, from where the voltages were increased to find the optimum. As explained above, the optimum could not be reached due to the limited output voltage of the voltage supplies.

To evaluate the data, I determined the signal amplitude for each spectrum by taking the maximal value. Then, I divided the values by the reference values for the corresponding frequency. The gain shows a steady slope w.r.t. V_{Drain} , without the plateau region being reached, as it appears to be at drain voltages $> 2\text{V}$, as shown in Fig. 12.

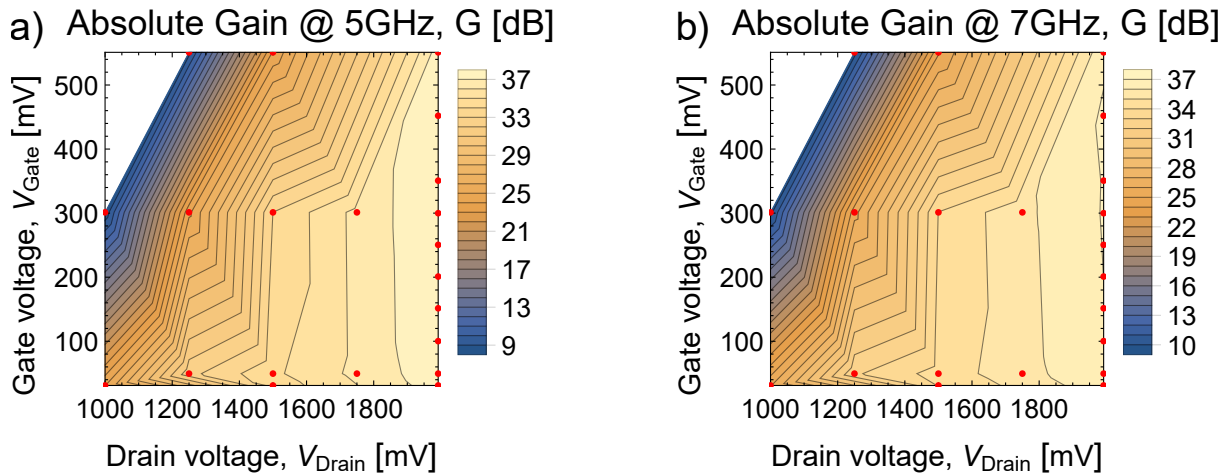


FIG. 12: The absolute gain measured for the HEMT in the circuit shown in Fig. 11 for the two investigated frequencies, 5 GHz (a) and 7 GHz (b). The red points again show the actual measurements.

4 Results & Discussion

4.1 Voltage decay

Assuming cabling with a resistance of R_{Cable} , and an amplifier with R_{Drain} resistance between drain input and ground (calculated from the specified drain voltage and current), and an infinite resistance between gate input and ground (a schematic of this is shown in Fig. 13), the voltages are

$$\begin{aligned} V_{\text{Drain}}^{\text{out}} &= \frac{R_{\text{Drain}} V_{\text{Drain}}^{\text{in}}}{2R_{\text{Cable}} + R_{\text{Drain}}} \\ V_{\text{Gate}}^{\text{out}} &= V_{\text{Gate}}^{\text{in}} - \frac{R_{\text{Cable}} V_{\text{Drain}}^{\text{in}}}{2R_{\text{Cable}} + R_{\text{Drain}}}. \end{aligned} \quad (4.1)$$

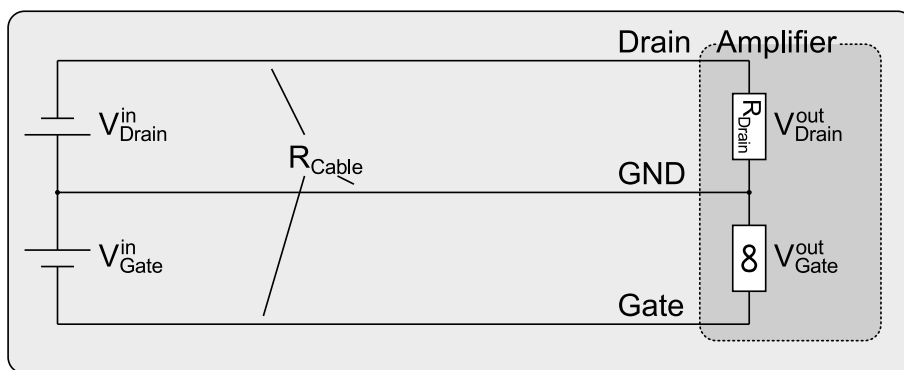


FIG. 13: Schematic of the DC cabling to one of the amplifiers. The circuit shown was used to derive Eq. (4.1).

Here, $V_{\text{Drain,Gate}}^{\text{in}}$ are the voltages applied at the input of the cryostat (i.e. the settings of the voltage supply) and $V_{\text{Drain,Gate}}^{\text{out}}$ are the voltages over the ports of the HEMT.

Accounting for this effect, the voltages that should be applied in the case of the first two experiments become $V_{\text{Drain}}^{\text{in}} = 0.58 \text{ V}$, $V_{\text{Gate}}^{\text{in}} = 0.36 \text{ V}$. Here, 2 m of cables with $2.3 \Omega/\text{m}$ were assumed, together with $R_{\text{Drain}} = 62.5 \Omega$ and specified voltages of $V_{\text{Drain}}^{\text{out}} = 0.5 \text{ V}$, $V_{\text{Gate}}^{\text{out}} = 0.35 \text{ V}$. The experimentally determined optimal bias voltages are even larger, $V_{\text{Drain}}^{\text{in,exp}} = 0.68 \text{ V}$, $V_{\text{Gate}}^{\text{in,exp}} = 0.46 \text{ V}$. This discrepancy can be accounted for by noting that the estimate above assumes perfect cabling, with no bad contact. Note that it is in principle straightforward to measure the resistance of the cable and HEMT and calculate the voltages to apply this way, removing the need to estimate the resistances.

The predicted voltages when considering this effect also match the results from the third experiment (section 3.3 on page 9): Assuming 1.9 m of cabling with $10 \Omega/\text{m}$ resistance and a resistance of 28Ω between the drain and ground ports of the HEMT at room temperature, the specified voltages of $V_{\text{Drain}} = 1.25 \text{ V}$ and $V_{\text{Gate}} = 0.05 \text{ V}$ correspond to 2.9 V and 0.9 V at the voltage supplies, which explains why the optimal settings could

not be reached.

5 Summary

I was able to demonstrate that significantly better performance (5–7 dB increase in gain, factor 2 decrease in noise temperature) can be achieved for the HEMT amplifier by optimizing the bias voltages. I also showed that the specified voltages are a good starting point when scanning for the optimal settings, assuming the voltage drops on the cabling leading up to the amplifier have been accounted for.

I was also able to demonstrate that it is possible to estimate the absolute gain and the noise temperature of a component in the signal processing circuit without having a reference line or having to modify the circuit.

6 Acknowledgements

I would like to thank professor Andreas Wallraff for allowing me to do this project in his group. Further, I would like to thank Theodore Walter and Philipp Kurpiers for supervising and guiding me throughout the project.

7 Bibliography

- [1] H. Nyquist. Thermal agitation of electric charge in conductors. *Physical Review*, 32(1):110–113, July 1928.
- [2] Chris Angove. What is the noise figure of a matched attenuator in thermal equilibrium? 2010. URL: http://www.chrisangove.com/ee_ref/attenNF_1b.pdf.
- [3] H.T. Friis. Noise figures of radio receivers. *Proceedings of the IRE*, 32(7):419–422, July 1944.

8 Appendix

A Voltage settings

V_{Drain}	V_{Gate}	V_{Drain}	V_{Gate}	V_{Drain}	V_{Gate}
0	0	520	560	720	600
480	320	560	360	720	640
480	340	560	400	760	400
480	360	600	440	760	520
480	400	600	640	760	560
480	760	640	480	760	600
500	300	680	340	800	560
500	320	680	460	800	640
500	340	680	520	840	480
500	360	680	560	840	680
520	320	680	600	880	720
520	360	720	520	920	300
520	400	720	560	920	760

TABLE I: The voltage settings investigated during the VNA and FPGA measurements.

V_{Drain}	V_{Gate}	V_{Drain}	V_{Gate}	V_{Drain}	V_{Gate}
680	520	680	460	740	400
700	520	640	460	720	500
660	520	640	480	720	500
660	500	680	480	720	500
680	500	680	510	720	500
700	500	660	510	700	440
640	500	640	510	680	440
620	500	680	515	720	440
600	500	680	518	700	440
580	500	680	525	700	440
720	500	680	520	740	440
660	480	700	520	660	480
660	460	660	520	660	480
660	440	720	420	660	480
620	440	700	420	500	320
700	440	720	460	720	560
				700	480

TABLE II: The voltage settings investigated during the second set of FPGA measurements, which are concentrated around $V_{\text{Drain}} = 680$, $V_{\text{Gate}} = 480$.

B DC Cabling

The DC cabling for Aphrodite is based on the DC cabling for BluFors 1. There are also 24 single lines, but they are distributed differently: 6 pairs are used for 6 coils, and the remaining 12 lines are used for 4 amplifiers with one gate voltage each (instead of 3 amplifiers with two gates each).

B.1 Breakout box

The breakout box is a RF tight aluminum box with two compartments, one noisy and one quiet, separated by a RF tight wall. The wall contains feedthrough filters (Tusonix 4601-050), one for each line. A schematic of the working principle can be seen in Fig. 14: The noisy compartment contains two/four-pole double throw switches (two poles for the coils, four for the amplifiers). In the 'on' position, the switch connects the input of the box to the cable going to the experiment, in the 'off' position, the cryo side is grounded to the box through a $1\text{ k}\Omega$ resistor for safe discharge. Since the box connects the shields on the input and output side, the input side shields should not be grounded.

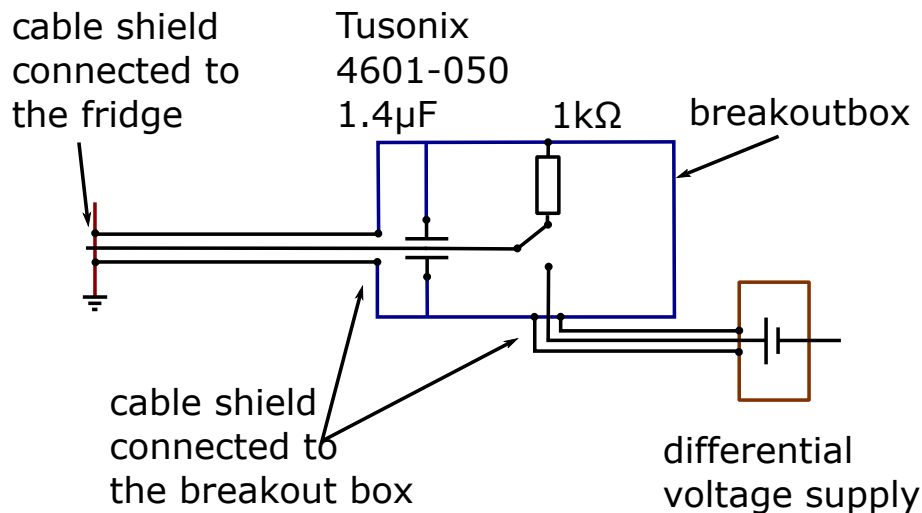


FIG. 14: Schematic of a single line of the DC breakout box. Shown is the voltage input (bottom right), the output (left) and the box itself containing the resistor (for discharge), the filter and the switch.

B.1.1 Cabeling

The layout of the switches as seen from the outside is shown in Table III. Note that the numbering of the switches does not match the numbering as seen on the labels (these were adjusted to match up with the first box).

FIG. 15 shows a schematic of the pin assignment for the D-Subs (30081.1 & 30081.5, D-Phys shop) connected to the voltage supplies for the amplifiers, the LEMO connectors (EGG.0B.302.CLL & FGG.0B.302.CLAD52Z (2 pin, coils) and EGG.0B.304.CLL &

HEMT 1	HEMT 2
A3	A4
HEMT 3	HEMT 4
A1	A2
COIL 1	COIL 2
C5	C6
COIL 3	COIL 4
C3	C4
COIL 5	COIL 6
C1	C2

TABLE III: Layout of the switches as seen from the outside of the box (output points towards the top). The top labels are the ones seen on the box, the bottom ones are the ones used internally.

FGG.0B.304.CLAD52Z (4 pin, amplifiers), LEMO) forming the input of the breakout box, and the switches for the coils and amplifiers. The cable colors correspond to the colors of the two/four-channel cable from the D-PHYS shop. Note that the brown lines for the amplifiers (Gate B) are terminated (not enough lines). The shield of the cables between D-Sub and LEMO are grounded on the box side, the cables from the switches to the filters are grounded on the switch side.

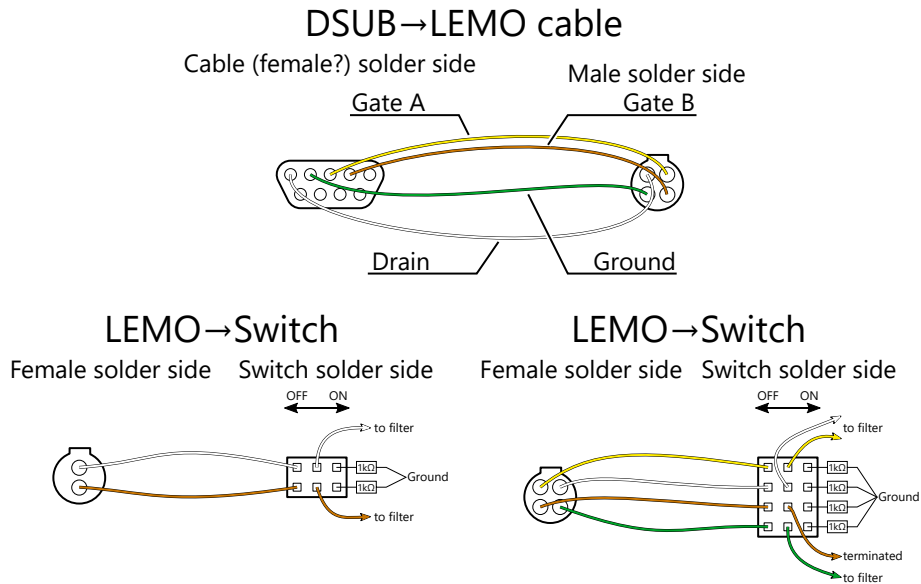


FIG. 15: Schematic of the input LEMO pin assignments, together with the schematic for the cable from the voltage supply to the breakout box for the amplifiers

The channel layout at the filter array is shown in Fig. 16. The color codes for the input side again correspond to the two/four-channel cables, the ones on the output side to

the 25-channel cable. The 25th channel (gray with red dots) is unused. This ordering (amplifiers at the bottom, coils on the top) was chosen since this means that the cables connecting the switches closest to the filter array (belonging to the amplifiers) are not too short.

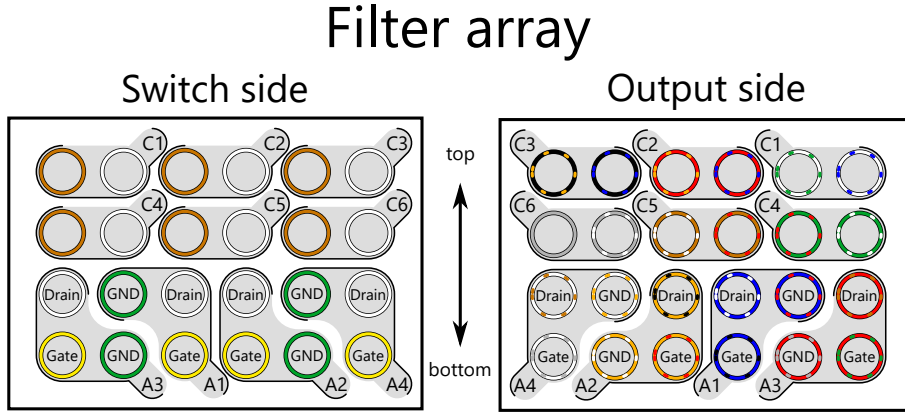


FIG. 16: Assignment of the filters in the wall separating the two compartments of the box. The color of the rings refers to the colors of the two/four channel cables on the input side and the 25 channel cable on the output sides. Note that "top" refers to the top of the box (where the switches are, which is the bottom when the box is open).

The channel assignment for the LEMO connector (FGG.3B.324 & HGG.3B.324, LEMO) on the output side of the breakout box is shown in Fig. 17.

Male solder side

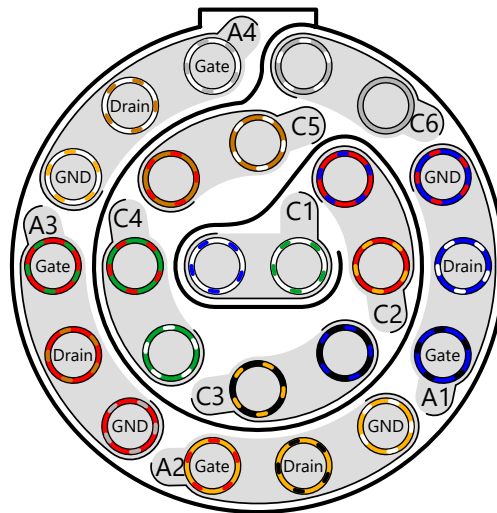


FIG. 17: Pin assignment for the 24-pin LEMO connector at the output cable of the breakout box. The color code used is again the one found on the cable.

B.1.2 Assembly

The soldering was done in the following order:

- Individual switches
 - Resistors
 - Cable to the filters (only switch side)
 - Cables to the input (only switch side)
 - Cable grounding shield
- Switch to input
- Mounted filters
- Switch to filters
- Output LEMO to cable
- Output cable to filters

B.1.3 Checks

The box has repeatedly been checked for cross connections to ensure proper functionality. The following has been checked:

- Nothing is connected to ground when ON
- Inputs not connected to ground when OFF
- Inputs not connected to outputs when OFF
- $1\text{ k}\Omega$ between outputs and ground when OFF
- Inputs connected to outputs when ON
- No interconnections when ON

B.2 DC cabeling

For the cabling from the input LEMO of the fridge to the D-Subs (micro D-Subs, [02-31-061](#) & [02-31-062](#), CMR-Direct) at the 4K stage, a 12-twisted-pair beryllium copper loom ([02-32-001](#), CMR-Direct) was used. The channel assignment for the loom and the pin assignment for the D-Subs (one for the coils and one for the amplifiers) is shown in [Fig. 18](#). Some effort was made to prevent damage on the loom connections: At the input, a PEEK tube (from the PHYS shop) of about 10 cm has been mounted onto the LEMO

connector. A schematic of this can be seen in Fig. 19. On the D-Sub side, the fabric of the loom was tied to the screws holding the D-Subs in place to reduce the amount of stress exerted onto the loom wires.

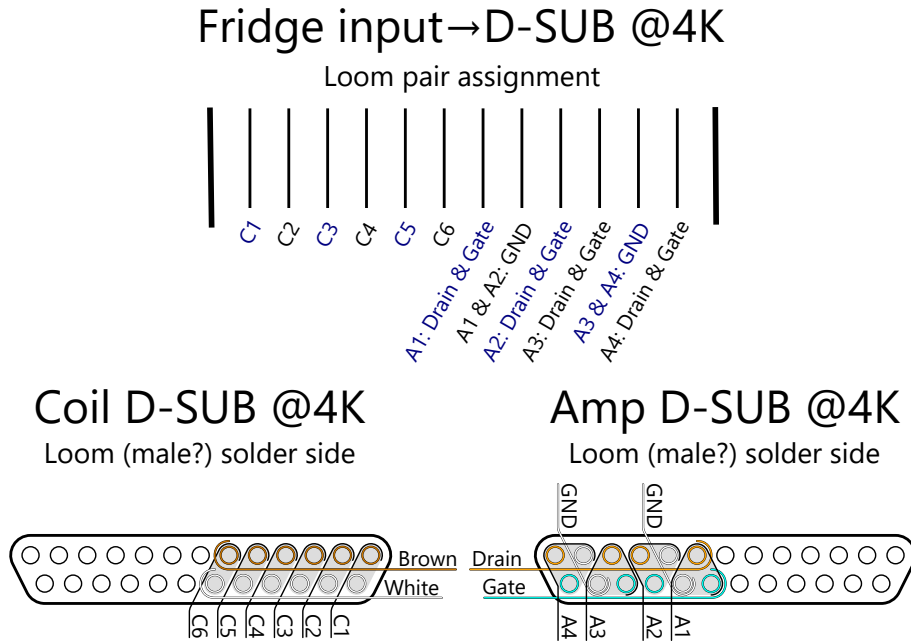


FIG. 18: Assignment of the twisted pairs of the loom and the pins of the micro D-Subs at the 4K stage.

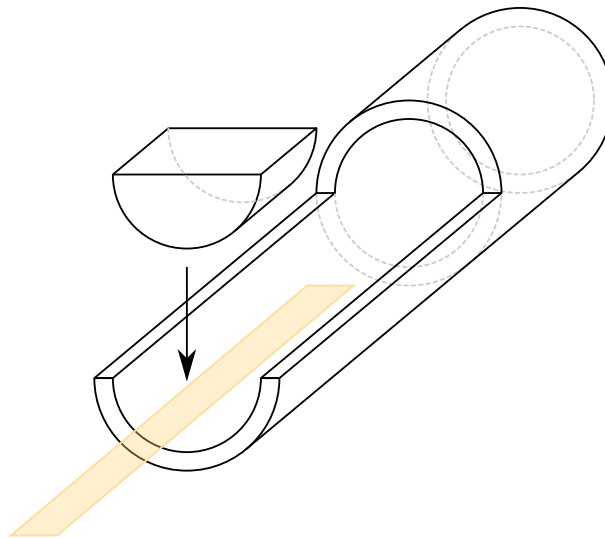


FIG. 19: Schematic of the loom protection at the LEMO connector at the cryo input. As can be seen, the loom is held in place by the half rod piece and the tube.

B.2.1 Interconnections

Two of the loom pairs appear to be slightly damaged and have had interconnections. The issue has been determined to be located at the thermalization clamp at the 4K stage and has been fixed by moving the problematic part of the loom outside the clamp.