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Read-Out Strategies for Multi-Qubit States in Circuit Quantum Electrodynamics

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Abstract

In cavity quantum electrodynamics (QED) experiments the interaction between single photons and atoms is studied. The analogous on-chip implementation – called circuit QED – uses superconducting electronic quantum circuits coupled to a co-planar transmission line resonator. It exhibits vastly enhanced coupling strengths between artificial atoms and microwave photons and therefore allows for studying novel quantum optical phenomena and experiments in the field of quantum information processing.

The main goal of this thesis is to implement an effective high performance single shot read-out of qubit states in a circuit QED setup. A field programmable gate array (FPGA) is programmed for fast signal processing and real-time analysis of the measurement signal. In contrast to the commonly used ensemble average measurement in circuit QED the implemented single shot projective measurement can be used for measurement feedback control and error correction. To infer whether the qubit is in its ground or excited state the quadrature components of the transmitted signal are integrated in each single experiment. To enhance the qubit read-out fidelity both the decision function used for inferring the qubit state and the integration time are optimised for the specific experimental parameters, such as measurement frequency, measurement power, qubit decay rate and photon decay rate. To evaluate the experimentally observed single shot performance a careful digital filter analysis and characterisation of the noise in the system is performed resulting in good agreement between experiment and theory. By means of single shot measurements the noise temperature of the amplifier chain, the cause of the rather low signal to noise ratio, is assessed. Furthermore, a framework for the integration of the FPGA in an existing measurement setup is established to simplify the control of the FPGA analysis. This work also forms the basis of further extensions to single shot multi-qubit read-out and to higher qubit level to increase the read-out fidelity.

Abstract

Preface

This diploma thesis was written externally at the Quantum Device Lab, Department of Physics, Laboratory for Solid State Physics of the ETH Zurich between June 2008 and June 2009. The document itself was written in LaTeX, and most figures were generated using the software program Mathematica.

There are several people I would like to thank.

I am deeply grateful to Prof. Dr. Andreas Wallraff of the ETH Zurich for proposing this interesting topic to me and for his excellent help and support. My thanks to Prof. Dr. Harald Weinfurter and Prof. Dr. Otmar Biebel for giving me the opportunity to write my thesis externally in the group of Prof. Dr. Andreas Wallraff.

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Zurich, June 2009
Christian Lang

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Chapter 1

Introduction

During the last decades the field of quantum information theory became very popular for applied quantum physicists. In contrast to classical information theory quantum information theory works with qubits instead of classical bits. The main difference to the classical bit is that the qubit does not need to be either 0 or 1 but can also be in a superposition of the states $|0\rangle$ and $|1\rangle$, restricted to the shell of the unit Bloch sphere. The possibility of a superposition, if utilised appropriately, leads to a speedup of some important algorithms. For example, the factorisation of a number N is classically of exponential complexity, but in quantum information theory an algorithm of complexity class $O(\log^3(N))$ in time and $O(\log(N))$ in quantum storage exists (Shor, 1997). Up to now the security of most cryptography algorithms is based on the fact that factorising the product of two large primes is classically of exponential complexity. Therefore a large scale quantum computer that is able to factorise the number N into its primes in time $O(\log^3(N))$ would make cryptography algorithms potentially insecure. With the advent of quantum information science 'quantum' cryptography is available. Here a one time pad, which consists of random numbers, is distributed to exactly two parties. Within the framework of quantum science it is proven that nobody else will get access to this one time pad, even a third party with infinite quantum mechanical power (Gisin et al., 2002). The one time pad can be used to cipher between the two parties with a security of 100 %. Quantum cryptography is the first application at the single quantum level (Gisin et al., 2002). There are more examples of a computational speed-up when using quantum computers, e.g. search applications over unsorted data. The Grover database search algorithm finds the desired entry in a database with N entries with only $O(\sqrt{N})$ queries (Grover, 1997) while classically $O(N)$ queries are needed.

There are several approaches to implement a quantum processor. Using nuclear magnetic resonance (NMR) quantum computing is performed on a whole bunch of molecules (Cory et al., 1997). In such a system the number 15 was factorised into 3 and 5 (Vandersypen et al., 2001) using Shor's quantum factoring algorithm (Shor, 1997). In terms of further scalability to much higher qubit numbers these systems are limited (Cory et al., 1997). Another approach is to trap cold ions in a linear Paul trap and use the states of the ions as qubits. The ions can be manipulated using laser beams. The collective centre of mass motion is used as a quantum bus which allows for a selective interaction between different qubits (Cirac and Zoller, 1995). Probably these systems are currently at the

most advanced level. However, they have some drawbacks like the restricted scalability of the ion number in the trap (even though there are ideas to bypass, see Kielpinski et al. (2002)) and the slow gate time (even though fast in comparison to the decoherence time). Other promising candidates include cavity quantum electrodynamics (QED) (Haroche and Raimond, 2006), quantum dots (Loss and DiVincenzo, 1998; Imamoglu et al., 1999), nitrogen vacancy centre (Childress et al., 2006), linear optics (Walther et al., 2005), etc. Our approach is a circuit QED system, an on-chip implementation of cavity QED using superconducting electronic quantum circuits. Here, artificial atoms embedded in a coplanar transmission line resonator exhibit vastly enhanced coupling strengths between artificial atoms and microwave photons in the resonator (Schoelkopf and Girvin, 2008).

Systems proposed for implementing a quantum computer have to fulfil the five (plus two) DiVincenzo criteria (DiVincenzo, 2000) to assess whether they are promising candidates for performing large scale quantum algorithms. The criteria are: 1) Is it a scalable system with well characterised qubits? 2) Is it possible to initialise the qubits before the start of the computation? 3) Is the decoherence time of the qubits much longer than the operation time? 4) Is a universal set of quantum gates accessible (controlled NOT and one qubit gates can model every multi qubit gate)? 5) Is it capable to perform qubit specific measurements? Further criteria are related to quantum communication: 6) Can flying and stationary qubits be interconverted? 7) Can flying qubits be transmitted? (DiVincenzo, 2000). The circuit QED (Blais et al., 2004) setup used in this work, a cavity QED setup fabricated on a chip using superconducting electric quantum circuits, fulfils the criteria. In contrast to most other systems the qubits are macroscopic objects fabricated on a chip. Therefore, the qubit position is fixed by design and they do not need to be trapped. The properties of these artificial atoms can be engineered and adapted to the experimental needs. Concerning the DiVincenzo criteria we notice the following: 1) The qubits are well characterised and several (in the order of ten) can be fabricated in the cavity at fixed places where they can be controlled individually. As in other systems the qubits can be in a coherent superposition of some states. Further scalability could be reached for example in a cavity grid (Helmer et al., 2009). 2) The system is initially automatically in its ground state $|00\ldots\rangle$ due to thermal relaxation. 3) The possible decoherence time in the order of 1–10 μs is high compared to the gate operation time of several ns (Blais et al., 2004). 4) Strong coupling between cavity and qubits is achieved due to larger dipole moments in contrast to cavity QED as a consequence of the one dimensional cavity (Blais et al., 2004). This enables the implementation of fast one and two qubit gates, which form a universal set of quantum gates as already demonstrated by DiCarlo et al. (2009). 5) The requirement for qubit specific measurements is fulfilled in that multi-qubit states can be distinguished in a joint dispersive read-out scheme (Filipp et al., 2009). 6) Flying qubits, here microwave photons, can transpose their state with the fixed qubits in the cavity and vice versa. 7) These photons can be transmitted via transmission lines to different locations. However, it is still a long way towards a large scale quantum processor, although up to now a number of fundamental experiments have successfully been performed: The strong coupling is reached (Wallraff et al., 2004), one qubit gates are well controlled (Wallraff et al., 2005), multiple qubits can be coupled via

virtual photons (Majer et al., 2007), due to the good understanding of the system the Lamb shift could be measured (Fragner et al., 2008), two qubit gates are demonstrated (Leek et al., 2009), the multi-qubit density matrix is measurable (Filipp et al., 2009), single qubit gate errors were characterised to be small (Chow et al., 2009) and basic algorithms were demonstrated (DiCarlo et al., 2009).

Circuit QED systems are one of the leading contenders for quantum information processing. One missing feature is a way to implement high-fidelity single-shot measurements, which would allow in contrast to the currently used ensemble average measurement for simplified quantum error correction (DiVincenzo, 2000). Quantum teleportation could be performed with direct feedback on the teleported qubit so that no postselection is necessary. To the best of my knowledge there is no quantum teleportation been reported without postselection but with direct single shot measurement feedback on the qubit. Single shot feedback on qubits has also never been demonstrated in the field of circuit QED.

The main goal of this thesis is to realise single shot measurements in a circuit QED setup. One requirement for direct feedback is that based on the measurement outcome unitary transformations on the qubits are completed within a fraction of the decoherence time. Since the decoherence time is in the order of μs, real-time signal analysis becomes a hard task for ordinary computers. For that reason a field programmable gate array (FPGA) has been implemented to perform single shot signal analysis. The signal analysis should be adaptable for future requirements, such as more advanced signal analysis, power averaging, correlation measurements, feedback tasks, etc. Additionally to the real-time measurement analysis an advantage of FPGA based signal processing is the reduced data storage space and data processing time. The digitised measurement signal is reduced to the outcome of the appropriate signal analysis. In addition processor time is saved as the signal processing is done by a highly parallel and specialised "digital circuit" on the FPGA, faster than any PC processor which performs computations sequentially. Using a programmable FPGA, the digital signal processing can be programmed to conform exactly our needs, in particular single shot signal analysis.

In course of this thesis I have programmed the FPGA to perform digital downconverting of a heterodyne signal, signal recording, signal averaging and single shot signal analysis. The control of the FPGA has been fully integrated into the existing control software. In order to set up a reliable system the signal processing performed by the FPGA is carefully analysed and the consistency with existing measurement routines has been verified. Additionally, noise and the signal to noise ratio of the experimental setup has been analysed. To achieve quantitative understanding of these figures, the gain of the amplifier chain behind the output port of the resonator has been measured and the noise temperature of the amplifier system has been worked out. Single shot read-out is performed using a projective transmission measurement by integrating the quadrature components of the measurement signal for each single shot on the FPGA. These integrals are used to decide whether the qubit is in its ground or excited state. This single shot measurement procedure is applied for qubit state read-out and compared to the theoretical expected performance showing good agreement to the experimental observed data. For further

improvements and extensions single shot measurements of higher excited qubit states and multi-qubit states are performed. A maximal single shot read-out fidelity for a single qubit of 73 % was observed.

Chapter 2 gives a short theoretical overview on the field of circuit QED in the relevant parameter regime. In Chapter 3 the experimental realisation and the measurement setup are presented. Afterwards, the FPGA and the software developed for its operation and its use are described in Chapter 4. A verification of the functioning of the FPGA and the consistency with existing measurement routines are given in Chapter 5. Chapter 6 theoretically discusses noise and its evolution during signal processing which is finally applied to analyse the noise temperature in the measurement setup. The theory of single shot measurements and experimental single shot measurements are presented in Chapter 7. The thesis closes with a summary and outlook, Chapter 8.

Chapter 2

Theory

In the following a short overview of the theory, that is necessary to understand the principles of the measurement and qubit control, is given. First the Jaynes Cummings Hamiltonian in terms of cavity quantum electrodynamics (QED) is introduced which is then adapted to meet our circuit QED system. The principle of the qubit state read-out by a transmission measurement is derived followed by the principle of the qubit control.

2.1 Cavity QED, Jaynes Cummings Hamiltonian

In the field of cavity QED the interaction between light confined in a cavity and atoms is investigated (Haroche and Raimond, 2006). The cavity consists of two highly reflecting mirrors between which photons can bounce back and forth several times before leaving the cavity. The distance between the mirrors defines the quantised electromagnetic field modes which allow only photons with certain frequencies to spend a long time in the cavity. In the cavity a two-level atom is placed whose state $|e\rangle$ is connected to state $|g\rangle$ by an electric dipole transition at angular frequency ω_a. Figure 2.1 shows this system consisting of a single mode and a single two level system schematically. The atom couples to the electromagnetic mode by an electric dipole interaction since the electromagnetic mode induces an electric dipole moment in the atom. In the case in which the photon

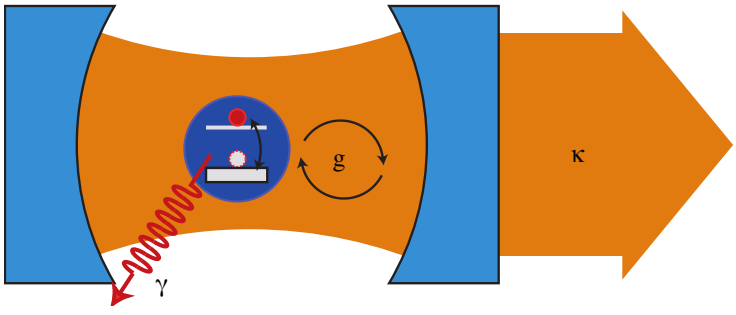


Figure 2.1: Typical cavity QED system. The electromagnetic field is confined by two highly reflecting mirrors (photon decay rate κ) and an embedded atom idealised as a two level system (spontaneous decay rate γ) coupled by the electric dipole interaction with strength g (Wallraff, 2008; Blais et al., 2004).

energy matches the energy difference between the two levels of the atom, single energy quanta are exchanged between the atom and the cavity field. This occurs at a rate g referred to as the coupling strength. Photons decay out of the cavity with rate κ and the atom decays spontaneously with a rate γ into other electromagnetic modes of the cavity or the environment (Blais et al., 2004).

The Jaynes Cummings Hamiltonian

$$H_{JCM} = \hbar\omega_r \left(a^\dagger a + \tfrac{1}{2}\right) + \tfrac{1}{2}\hbar\omega_a\sigma_z + \hbar g \left(a^\dagger\sigma^- + \sigma^+ a\right) + H_\kappa + H_\gamma \tag{2.1}$$

describes such a system comprising a single electromagnetic field mode coupled to a single atom which is idealised as a two level system. The photon energy is $\hbar\omega_r$ and $\hbar\omega_a$ is the energy difference between ground ($|g\rangle$) and excited ($|e\rangle$) state of the two level system (Blais et al., 2004). The energies $\hbar\omega_a$ and $\hbar\omega_r$ can also be expressed in terms of the atom transition frequency $\nu_a = {}^{\omega_a}/_{2\pi}$ and the bare cavity resonance frequency $\nu_r = {}^{\omega_r}/_{2\pi}$, respectively. The first term in Equation (2.1) is the energy stored as photons in the cavity similar to the usual quantum mechanical harmonic oscillator. Here $a^\dagger$ denotes the creation operator of a photon with frequency ω_r in the cavity, which is defined as $a^\dagger |n\rangle = \sqrt{n+1}\,|n+1\rangle$ such that a photon is created in addition to the n existing photons. Similarly the photon annihilation operator a is defined as $a\,|n\rangle = \sqrt{n}\,|n-1\rangle$. Together they form the photon number operator $\hat{n} = a^\dagger a$ as $\hat{n}\,|n\rangle = a^\dagger a\,|n\rangle = a^\dagger\sqrt{n}\,|n-1\rangle = n\,|n\rangle$.

The second term in the Jaynes Cummings Hamiltonian (Equation (2.1)) describes the energy stored in the two level atom. The Pauli operator σ_z refers to the ground state $|g\rangle$ and the excited state $|e\rangle$ of the two level system with transition energy $\hbar\omega_a$ defined as $\sigma_z = |g\rangle\langle g| - |e\rangle\langle e|$.

The interaction between the field and the two level system is described by the third term in Equation (2.1). Single energy quanta are exchanged with rate g. A transition $\sigma^- = |g\rangle\langle e|$ from state $|e\rangle$ into state $|g\rangle$ of the atom emits a photon $a^\dagger$ into the respective cavity mode. In the case the photon gets absorbed ($\sigma^+ = |e\rangle\langle g|$) by the atom, a photon in the cavity is annihilated by a.

The coupling of the cavity to the continuum and the coupling of the atom to other modes than the single cavity mode is described by the fourth and fifth term, H_κ and H_γ, of the Jaynes Cummings Hamiltonian (Equation (2.1)) respectively (Blais et al., 2004). H_κ models the photon decay rate $\kappa = {}^{\omega_r}/_{Q}$. Here Q is the dimensionless quality factor of the cavity commonly defined as $Q = {}^{\nu_r}/_{2\delta\nu_r}$ with ν_r the cavity resonance frequency and $\delta\nu_r$ the half width half maximum (HWHM) of the Lorentzian line shaped cavity power transmission. H_γ leads to a spontaneous decay rate γ of the atom from state $|e\rangle$ into $|g\rangle$.

2.2 Circuit QED

In circuit QED the cavity QED system is implemented using superconducting electric quantum circuits as proposed by Blais et al. (2004) and experimentally realised by Wallraff et al. (2004). In the further sections of this chapter the presented theory will mainly

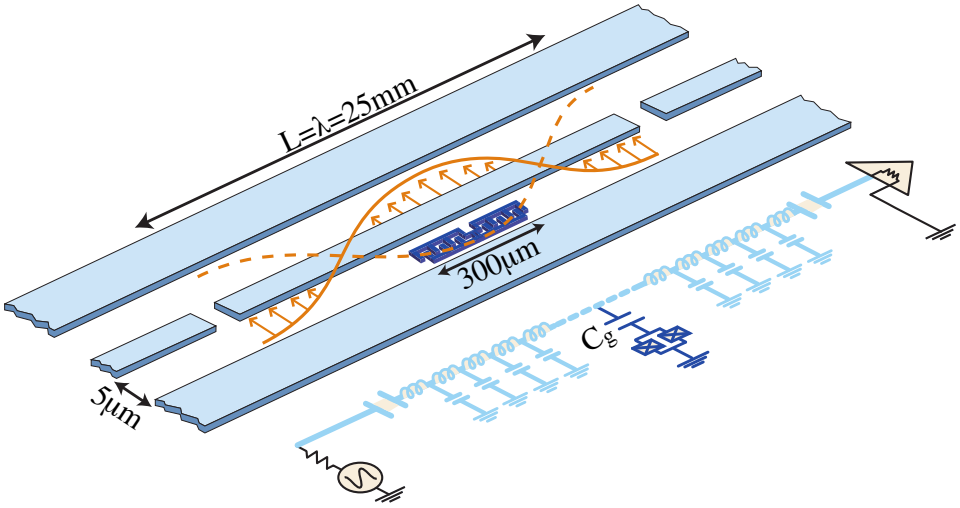


Figure 2.2: Schematic picture of the circuit QED system used in the following experiments. The system consists of a superconducting coplanar waveguide resonator (light blue) and a split Cooper pair box placed (dark blue) at an antinode of a standing wave (Blais et al., 2004). The transmission line resonator is coupled capacitively to the input and output lines. An equivalent lumped element circuit is shown below the schematic picture. Here the Josephson tunnel junctions used to form the split Cooper pair box are represented by crosses in a square. The transmission of the cavity is probed by irradiating microwaves to the input and amplifying the output to detect the signal. Picture from Wallraff (2008).

follow the proposals of Blais et al. (2004) and Blais et al. (2007) with extensions due to a qubit modification proposed by Koch et al. (2007). Figure 2.2 shows schematically the circuit QED system used in our laboratory. The cavity is replaced by a superconducting coplanar stripline resonator consisting of a centre conductor and two lateral ground planes. The length of the resonator and the effective dielectric constant ε^{eff} define the resonance frequency ν_r of the resonator (typically some GHz). Due to the use of superconducting material the resonator is nearly lossless. The ground planes confine the resonator mode laterally very strongly leading to a very high electromagnetic field strength in the resonator plane, i.e. a quasi one dimensional transmission line (Wallraff, 2008; Blais et al., 2004). At the input and output the resonator is coupled capacitively to conventional microwave transmission lines reproducing the continuum in cavity QED systems. The capacitors that couple transmission lines and resonator represent the mirrors in standard cavity QED systems.

The atoms in cavity QED systems are replaced by superconducting split Cooper pair boxes, placed at an antinode of the standing wave in the resonator where the highest electromagnetic field strength is located. The split Cooper pair box consists of a superconducting island and a superconducting reservoir that are connected by two (*split* Cooper pair box) Josephson tunnel junctions. The charging energy of single charges on the superconducting island is given by $E_c = {}^{e^2}/_{2C_\Sigma}$ where C_Σ is the sum of the following capacitances: capacitance via the Josephson junctions, capacitance from island to reservoir via an additional finger capacitor (compare Figure 2.2 or – for a more detailed view

– Figure 3.2), the effective capacitance to the resonator (C_g in Figure 2.2). Cooper pairs can tunnel through the Josephson junction from the reservoir to the island and back without loss. Since Cooper pairs have a macroscopic wave function a coherent tunnel current results which is influenced by the Josephson energy $E_J(\Phi) = I_c(\Phi)\,{}^{\Phi_0}/_{2\pi}$ (describing the potential barrier over the Josephson junctions), where Φ_0 is the flux quantum and $I_c(\Phi)$ is the critical current of the Josephson junctions. Through the ring that is formed by connecting the superconducting island to the reservoir by the first Josephson junction and the reservoir back to the island by the second Josephson junction the Josephson energy can be tuned by applying an external flux Φ as $E_J = E_{J,\max}\,|\cos(\pi\,{}^{\Phi}/_{\Phi_0})|$ (Makhlin et al., 2001). The Hamiltonian describing the split Cooper pair box on the basis of the number of Cooper pairs M that are on the island is given by

$$H_{\mathrm{CPB}} = 4E_c \sum_M (M - M_g)^2 \,|M\rangle\,\langle M| - \tfrac{1}{2}E_J \sum_M (|M+1\rangle\,\langle M| + |M\rangle\,\langle M+1|),$$

where $M_g = {}^{C_g V_g}/_{2e}$ is the dimensionless gate charge V_g (voltage applied between the centre conductor and the ground planes of the resonator) (Blais et al., 2004). In the regime $E_c \gg E_J$ the split Cooper pair box is referred to as a charge qubit, because the Hamiltonian is mostly defined by the number of Cooper pairs M on the island (Blais et al., 2004). In our experiments we use a refined version of the split Cooper pair box which is insensible to M_g gate charge fluctuations of the cost of reduced anharmonicity which still remains sufficiently large (Koch et al., 2007). The main difference is a reduced E_c where the split Cooper pair box is referred to as transmon in the regime $E_c \ll E_J$ (Koch et al., 2007). The class of phase qubits have even higher $E_J \sim 10^4 \cdot E_c$ and are usually arranged in a different way (Makhlin et al., 2001).

For the case in which the transmon is placed at an antinode of the standing wave in the resonator, transmon and electromagnetic field in the resonator couple by electric dipole interaction. The Hamiltonian for this system in the uncoupled transmon state basis is the generalised Jaynes Cummings Hamiltonian (extended to more than two levels of the atom)

$$H = \hbar\omega_r \left(a^\dagger a + \tfrac{1}{2}\right) + \sum_i \hbar\omega_i \,|i\rangle\,\langle i| + \sum_{i,j} \hbar g_{i,j} \,|i\rangle\,\langle j|\,(a^\dagger + a), \tag{2.2}$$

where index i and j run over all transmon states $i, j = g, e, f, h, \ldots$; ω_i is the transition frequency from state $|g\rangle$ to $|i\rangle$ and $g_{i,j}$ is the coupling strength to absorb or emit a photon caused by a transition of the transmon from $|i\rangle$ to $|j\rangle$ (Koch et al., 2007). In principal, any quantum mechanical two level system can be used as a qubit in quantum information theory. The two level system of our choice is given by the $|g\rangle$ and $|e\rangle$ state of the transmon and is referred to as qubit in the further thesis. The generalised Hamiltonian can be approximated appropriately, as done in the following section, to an effective two level system for the transmon states $|g\rangle$ and $|e\rangle$. The resulting effective Hamiltonian then describes the qubit (or even more than one qubit) coupled to the cavity.

2.3 Dispersive read-out

The detuning of the transmon state $|i\rangle$ from the resonator is denoted by $\Delta_i = \omega_{i,i+1} - \omega_r$, where $\omega_{i,j}$ is the transition frequency of the transmon state $|i\rangle$ to $|j\rangle$. Usually, experiments are performed in the dispersive regime, that is, in the case where the transmon is operated at transition frequencies where $g_{g,e} \ll |\Delta_g|$ (Koch et al., 2007). Due to the reduced anharmonicity in the transmon (in comparison to the Cooper pair box device) more than the first excited state needs to be taken into account. Virtual transitions through higher excited states lead to the effective dispersive Hamiltonian

$$H_{\text{eff}}^D = (\tfrac{1}{2}\hbar\omega_a')\,\sigma_z + (\hbar\omega_r' + \hbar\chi\sigma_z)\,a^\dagger a \tag{2.3}$$

$$= (\tfrac{1}{2}\hbar\omega_a' + \hbar\chi a^\dagger a)\,\sigma_z + (\hbar\omega_r')\,a^\dagger a, \tag{2.4}$$

for the restricted two-dimensional transmon Hilbert space with basis states $|g\rangle$ and $|e\rangle$ (Koch et al., 2007). Here, the qubit transition frequency $\omega_a' = \omega_{g,e} + \chi_{g,e}$ and the cavity resonance frequency $\omega_r' = \omega_r - \chi_{e,f}/2$ are renormalised as consequence of the restriction to the two-dimensional transmon Hilbert space. The effective dispersive shift χ is given by $\chi = \chi_{g,e} - \chi_{e,f}/2$ with $\chi_{i,j} = g_{i,j}^2/(\omega_{g,e} - \omega_r)$ leading to

$$\chi = -g^2 \frac{E_c/\hbar}{\Delta_g(\Delta_g - E_c/\hbar)},$$

where $g = g_{g,e}$ (Koch et al., 2007).

The second form of the effective dispersive Hamiltonian (Equation (2.4)) illustrates the AC-Stark shift of the transmon transition frequency. Each photon $a^\dagger a$ in the cavity shifts the transmon transition frequency by χ. Equation (2.4) can be obtained from Equation (2.3) due to the fact that the order of σ_z and $a^\dagger a$ can be reversed as they act on different states, namely the transmon state and the photon number state of the cavity, respectively.

The effective dispersive Hamiltonian in Equation (2.3) shows that there is a shift of the cavity resonance frequency of $\pm\chi$ depending on the transmon state $|g\rangle$ or $|e\rangle$ as $\sigma_z|g\rangle = (|g\rangle\langle g| - |e\rangle\langle e|)|g\rangle = |g\rangle$ and $\sigma_z|e\rangle = -|e\rangle$. A measurement of the cavity resonance frequency is a quantum nondemolition (QND) measurement of the transmon state because the operator σ_z is probed by measuring the cavity resonance frequency and σ_z commutes with H_{eff}^D ($[\sigma_z, H_{\text{eff}}^D] = 0$), which is therefore a constant of motion (Blais et al., 2004). A complex superposition $a|g\rangle + b|e\rangle$ ($|a|^2 + |b|^2 = 1,\ a, b \in \mathbb{C}$) collapses with probability $|a|^2$ or $|b|^2$ into the state $|g\rangle$ or $|e\rangle$ respectively, as soon as the state of the resonator field is determined. Further consecutive measurements of the cavity resonance frequency give the same results. However, the spontaneous qubit decay rate γ is still present preventing us to reach arbitrary large measurement accuracy (Blais et al., 2004). The shift of the cavity resonance frequency is illustrated in Figure 2.3.

To measure the transmon state a coherent microwave signal is irradiated at the input of the cavity and the quadrature components of the microwave signal transmitted through the

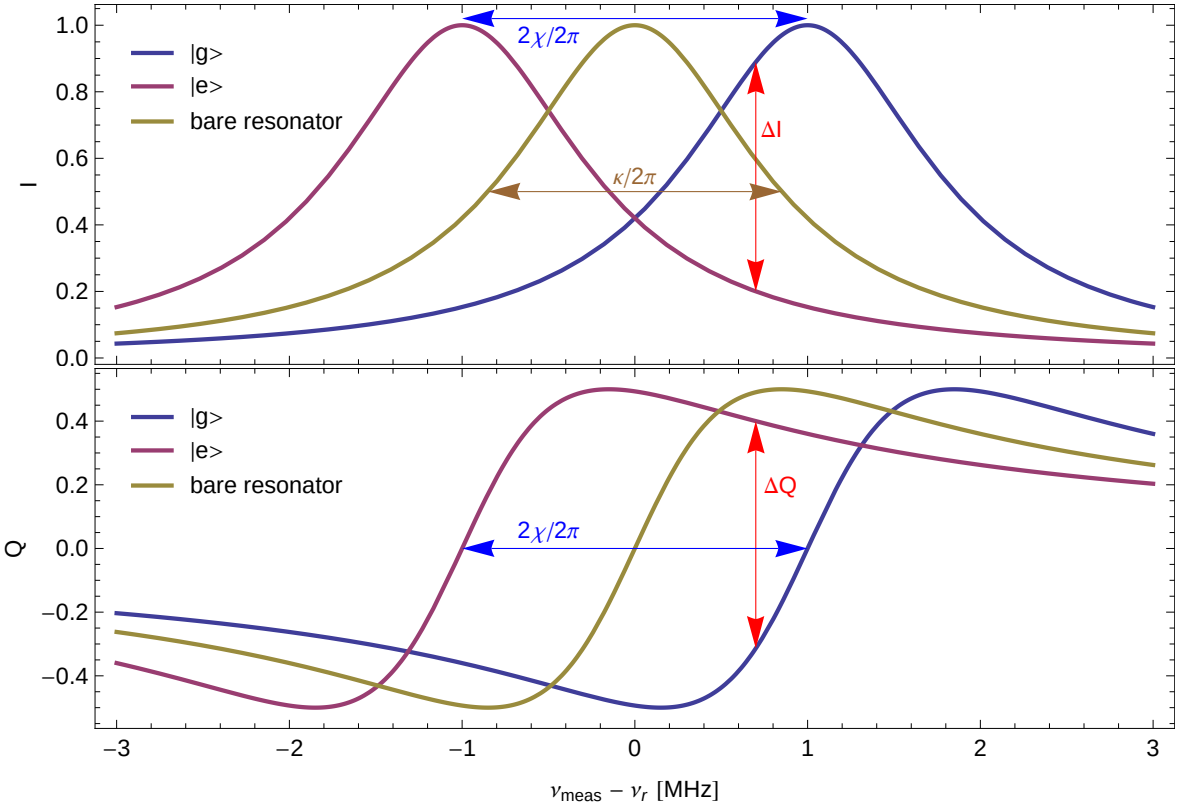


Figure 2.3: Schematic illustration of dispersive cavity resonance frequency shifts. The cavity resonance frequency is shifted by $-\chi$ with respect to the bare resonator frequency $\nu_r = {}^{\omega'_r}/_{2\pi}$ if the transmon is in state $|e\rangle$ and by χ if it is in $|g\rangle$, depicted by the blue arrows. The transmitted quadrature signal is shown as a function of the measurement frequency ν_{meas} in the steady state limit (constant measurement drive and fixed transmon state) for the transmon being in state $|g\rangle$, state $|e\rangle$ and without state dependent cavity shift ($\hbar\chi\sigma_z$, bare resonator), respectively (Filipp et al., 2009). An effective dispersive shift ${}^{\chi}/_{2\pi} = -1\,\mathrm{MHz}$ and the cavity decay rate ${}^{\kappa}/_{2\pi} = 1.7\,\mathrm{MHz}$ resulting in a nonzero width of the resonator (depicted by the brown arrow) were used in this example. From the difference (shown by the red arrows for $\nu_{\mathrm{meas}} - \nu_r = 0.7\,\mathrm{MHz}$) of the cavity transmission quadrature signal I and Q (top: I, bottom: Q) ΔI or ΔQ or any function of them, the cavity resonance frequency namely the transmon state can be inferred.

cavity are analysed. The Hamiltonian in the dispersive regime including the measurement drive is given by

$$H = H_{\mathrm{eff}}^{D} + \hbar\epsilon(t)\,(a^\dagger e^{-i\omega_{\mathrm{meas}}t} + a e^{+i\omega_{\mathrm{meas}}t}),$$
$$H' = (\tfrac{1}{2}\hbar\omega'_a)\,\sigma_z + (\hbar\omega'_r - \hbar\omega_{\mathrm{meas}} + \hbar\chi\sigma_z)\,a^\dagger a + \hbar\epsilon(t)\,(a^\dagger + a),$$

where $\epsilon(t)$ is the drive amplitude and H' is in the rotating frame with the measurement frequency ω_{meas} (Blais et al., 2004; Filipp et al., 2009). The quadrature of the homodyne

voltage at the output of the cavity is given by

$$I(t) = \sqrt{R\hbar\omega_{\text{meas}}\kappa}\,\Re(\langle a(t)\rangle), \qquad Q(t) = \sqrt{R\hbar\omega_{\text{meas}}\kappa}\,\Im(\langle a(t)\rangle),$$

with the impedance R at the output of the resonator (Bianchetti et al., 2009; Blais et al., 2004; Walls and Milburn, 2008). Figure 2.3 shows the steady state solution for the quadrature signal I and Q as a function of the measurement frequency $\nu_{\text{meas}} = {}^{\omega_{\text{meas}}}/_{2\pi}$. It can be clearly seen how the transmission measurement allows to conclude on the transmon state. The transmitted quadrature signal differs by ΔI and ΔQ in dependence of the transmon state. The transmon state can be inferred by analysing either I or Q or any function of them. In this thesis the quadrature signal is often denoted as $I + i\,Q$ because in the experiment I and Q are not fixed but are allowed to be rotated by a global phase offset φ_0 to $I' = \Re((I + i\,Q)\,e^{2\pi i\,\varphi_0})$ and $Q' = \Im((I + i\,Q)\,e^{2\pi i\,\varphi_0})$, where $\Re$ and $\Im$ denote the real and imaginary part respectively.

2.4 Qubit control in the dispersive regime

In quantum information processing it is crucial to have good one-qubit control. Here this is performed by driving the qubit by a microwave field with frequency at or close to the qubit transition frequency ω_a'. To model the effect of the qubit drive, the drive is added to the Jaynes Cummings Hamiltonian (Equation (2.1)) and the dispersive transformation is applied neglecting damping similarly as it was done to model the measurement drive but now with frequency ω_d (Blais et al., 2004). Since the qubit drive is substantially detuned from the resonator frequency ω_r', just a small fraction of the drive enters the cavity and can be considered as classical field (Blais et al., 2007). A time-dependent displacement transformation is applied to eliminate direct drive on the resonator. This results in the effective Hamiltonian

$$H^d = (\hbar\omega_r' - \hbar\omega_d)\,a^\dagger a + (\tfrac{1}{2}\hbar\omega_a' - \tfrac{1}{2}\hbar\omega_d + \hbar\chi(a^\dagger a + \tfrac{1}{2}))\,\sigma_z + \tfrac{1}{2}\hbar\Omega_R\,\sigma_x,$$

where $\Omega_R = 2\,\frac{\epsilon g}{\omega_r' - \omega_d}$ is the Rabi frequency at which the state vector of the qubit rotates around the x-axis in the Bloch sphere (Blais et al., 2007). By choosing other phases of the driving microwave signal, the axis, around which the state vector rotates, is chosen (any axis between x-axis and y-axis can be selected). The length T of the microwave pulse specifies the angle about which the state is rotated. Irradiating the qubit drive for time $T = \frac{1}{\Omega_R/2\pi}$ performs a π-pulse on the qubit. More precisely it transforms the qubit from $|g\rangle$ to $|e\rangle$. A pulse of $T = \frac{1/2}{\Omega_R/2\pi}$ produces a $\pi/2$-pulse which transforms the qubit initially in state $|g\rangle$ into an equal superposition $1/\sqrt{2}(|g\rangle + |e\rangle)$ of the two states of the qubit. A closer look on the Rabi frequency shows that it scales linearly with the drive amplitude ϵ providing another possibility to adjust the rotation angle (Blais et al., 2007). Each one-qubit gate can be performed by adjusting the qubit drive phase and the pulse length (or alternatively the drive amplitude).

Chapter 3

Measurement

This chapter deals with the experimental setup on which this work is based. In the first section the physical implementation of the circuit QED system is presented. Then, the measurement setup and the mounting of the circuit QED system in a cryostat is described. Further, a closer look on qubit control, pulse generation and transmission signal analysis is given. The last section introduces the time evolution of the transmission measurement signal.

3.1 Sample

The circuit QED system (compare Section 2.2) is implemented on a chip referred to, in the following, as "the sample". The sample was fabricated by Göppl (2009) and introduced schematically in Figure 2.2. The resonator is made from niobium and manufactured via optical lithography and etching on a monocrystalline sapphire chip (Göppl, 2009). To achieve a resonator frequency in the order of $\omega_r \sim 6\,\mathrm{GHz}$ the strip line resonator needs to have a length of about 25 mm. However, the sample chip has only a size of $2\,\mathrm{mm} \times 7\,\mathrm{mm}$. To fit the resonator on the sample chip the resonator is therefore wiggled in the centre of the chip where no qubits are placed. A microscope picture of the sample, most of my experiments are performed on, is shown in Figure 3.1. To connect the sample to

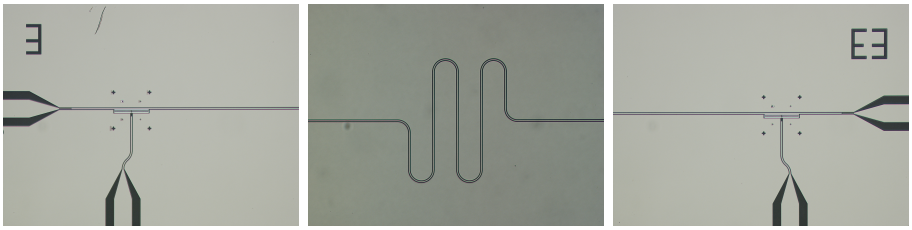


Figure 3.1: One circuit QED chip with two qubits produced and described by Göppl (2009). Left: Impedance matched inputs to the chip and input capacitor in the centre conductor (too small to see) to the cavity. Qubit A is placed between the centre conductor and the ground planes with the gate line capacitively coupled to it. Centre: Centre of the strip line resonator continued to the left and right pictures. It is wiggled around to fit the cavity on the chip. Right: Analogous to the left picture but with qubit B and the output of the cavity.

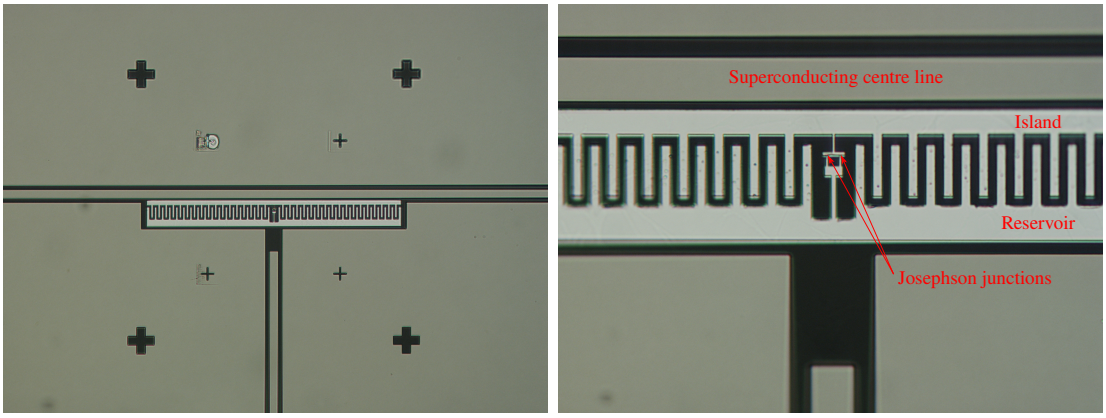


Figure 3.2: Qubit B (see Figure 3.1) placed in a strip line. The gate line capacitively coupling to the qubit is also shown. Black areas represent isolating layers, middle dark areas superconducting Niobium and light grey areas superconducting aluminium forming the island (top) and the reservoir (bottom). Island and reservoir are separated by the finger capacitor. Left: Picture of the whole transmon structure. Between the two horizontal isolating (black) lines the superconducting centre line (middle dark) can be seen. Right: Zoom into the SQUID (superconducting quantum interference device) area with the two Josephson junctions connecting reservoir and island of the split Cooper pair box. Island and reservoir are connected by the small structure in the centre where two vertical lines rest on the horizontal line (close to the island) with an isolating layer (aluminium oxide) in between. The overlaps between vertical lines and the horizontal line form the Josephson junctions which have a size in the order of 200 nm × 200 nm. Pictures and sample were produced by Göppl (2009).

conventional transmission lines the inputs on the chip are scaled down to the width of the strip line resonator keeping the commonly used impedance of $R = 50\,\Omega$ to avoid reflections at the input and output of the chip.

The qubits (transmons) are made from aluminium and aluminium oxide (for the isolating layer forming the Josephson junctions) and manufactured via electron beam lithography (to write smaller structures than possible with optical lithography) and shadow evaporation. Figure 3.2 shows microscope pictures of the right qubit B of Figure 3.1. The largest component (some 100 μm long) that forms the qubit is the finger capacitor, which ensures a large capacitance between island and reservoir, compare Section 2.2. The Josephson junctions are the smallest structures in the sample. Each Josephson junction consists of a small overlapping region of two superconducting fingers with a very thin isolating layer in between that allows Cooper pairs to tunnel through. The two fingers are connected to the island and reservoir respectively via superconducting aluminium.

The whole sample is connected and grounded to a sample holder by bond wires. The sample holder connects the input and output lines to adaptors where conventional transmission lines can be connected to. On the sample holder two superconducting coils are mounted close to the two qubits. The coils produce a controlled magnetic flux through the ring formed by the Josephson junctions, island and reservoir. The superconducting current through the ring protects against fluxes through the ring that are greater or equal

to the flux quantum Φ_0. However, the fraction of the flux which is smaller than Φ_0 can enter the ring and tunes the qubit transition frequency ω_a, compare Section 2.2. By adjusting the current through the two coils both qubits can be tuned independently to different qubit transition frequencies.

The gate lines were designed by Steffen (2008). They allow independent qubit drives (for one-qubit gates, compare Section 2.3) for the two qubits as a microwave drive going through a gate line couples very weakly into the cavity and therefore influences the second qubit only marginally. Microwave drives allow one-qubit operations as discussed in Section 2.3 as well through the gate line but with different coupling strength g in the Rabi frequency Ω_R. Coupling is here only possible to the qubit that is close to the gate line and therefore in the influence region of the microwave drive.

The qubit circuit QED sample has the following main parameters. The cavity resonance frequency is $\nu_r \approx 6.443\,\mathrm{GHz}$ and the decay rate $\kappa/2\pi \approx 1.7\,\mathrm{MHz}$. A vacuum Rabi mode splitting experiment determined the coupling strength to $g/2\pi \approx 134\,\mathrm{MHz}$. The charging energy is $E_c/2\pi\hbar \approx 230\,\mathrm{MHz}$ (Bianchetti et al., 2009).

3.2 Measurement setup

The sample is placed in a dilution refrigerator (cryostat) to be cooled down to temperatures at which the materials (aluminium and niobium) are superconducting and lossless. Additionally the resonator needs to be cooled down to avoid thermal photons $\langle n \rangle$ in the resonator:

$$\langle n \rangle = \frac{1}{e^{\hbar\omega_r/k_B T} - 1} \sim 10^{-6}$$

where ω_r is in the order of $5\,\mathrm{GHz}$ and $T < 20\,\mathrm{mK}$ the temperature to which the dilution refrigerator is able to cool down. The low temperatures are reached by using the evaporation heat of He^3 from a He^3-He^4-mixture. The measurement setup at the different temperature stages in the dilution refrigerator and its components that are outside the fridge at room temperature are shown in Figure 3.3.

The sample holder with the mounted coils is located at the base temperature stage of the refrigerator. The Bias T's allow to apply both microwave field and DC offset (bias) to the transmission lines by combining them in the base temperature stage of the cryostat. This is important because the bias needs to be extremely low pass filtered to achieve a low noise bias at the lines to the sample (on-chip) and to attenuate the microwave lines ordinary. The attenuator in the microwave lines to the sample filters out noise arriving from warmer parts, mainly parts with room temperature. A signal with high power can be sent to the refrigerator. It is attenuated until nearly no noise remains and the desired signal power is reached at the input to the sample. The attenuators and filter between the transmission lines also are used to thermalise the centre conductor of the transmission lines. The circuit QED sample (on-chip) in Figure 3.3 is shown in form of a lumped element circuit. The cavity is modelled as a LCR-circuit capacitively (over C_{in} and C_{out}) coupled to the input and output lines respectively. The qubits are modelled

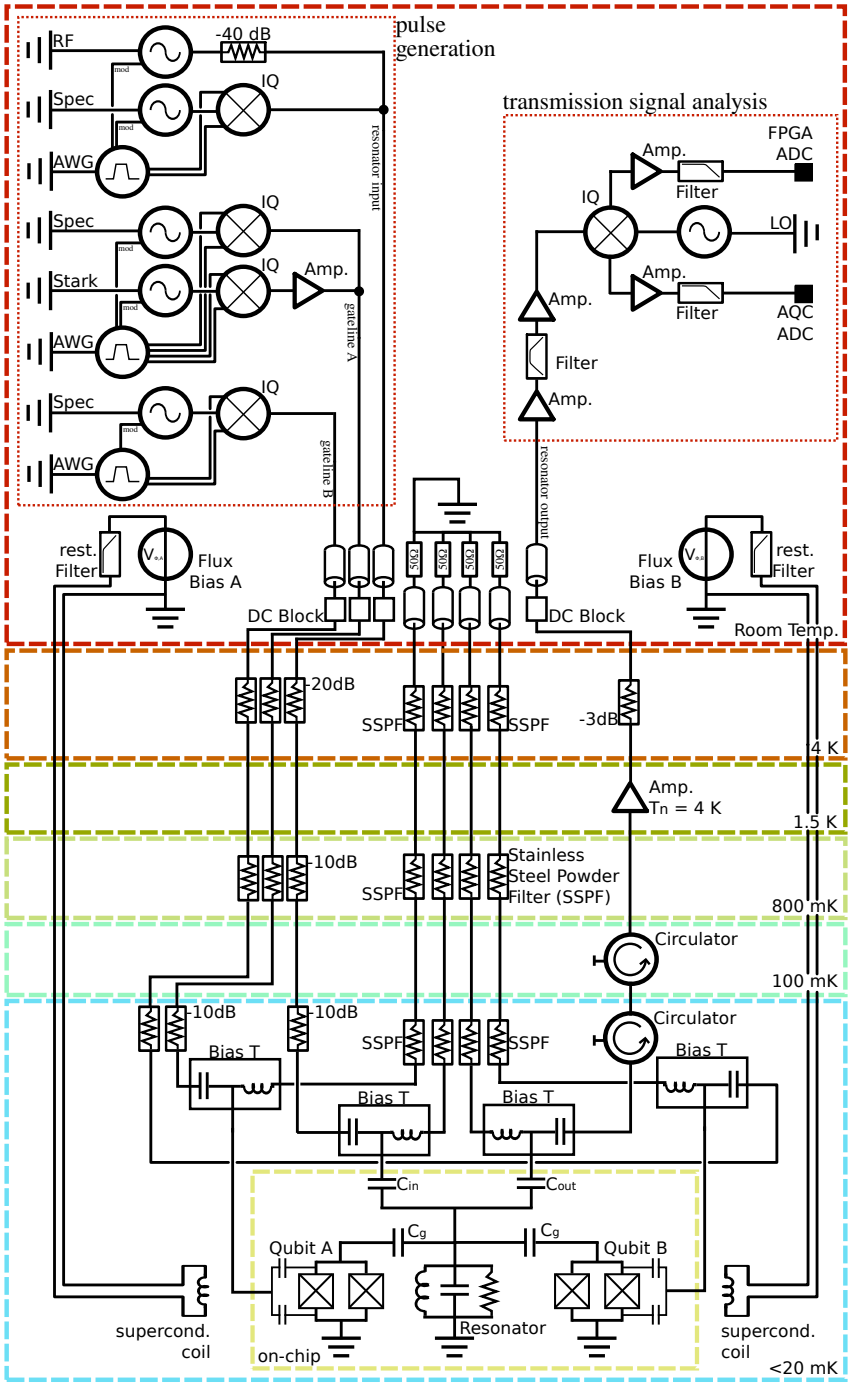


Figure 3.3: Overall measurement setup. The circuit QED sample is mounted in a dilution refrigerator with $\approx 17\,\mathrm{mK}$. Microwave transmission lines with low pass filter, attenuators, a low noise cold amplifier and circulator connect the circuit QED sample with the room temperature electronics through the different temperature stages of the refrigerator (orange to light blue). The room temperature electronics (red) consist of: Microwave pulse generator for coherent measurement and qubit control (left); Transmission signal amplifier, filter and digital to analog converter (right); DC qubit tuner (bottom). Parts of the figure were taken from Steffen (2008).

by the two Josephson junctions (crosses in a square), the island (top wire) and reservoir (bottom wire) coupling capacitively over C_g to the resonator. Flux through the qubit ring is applied by the nearby superconducting coil. Microwaves couple capacitively through the gate lines to island and reservoir modelled by the capacitors on the sides of the qubits (Steffen, 2008). The signal leaving the resonator at C_{out} needs to be amplified. The signal passing the "Bias T" to the RF-line can therefore not be attenuated (as done in the input lines) with the consequence that thermal noise can enter the resonator over C_{out}. Hence, two circulators are included in the setup to avoid entering thermal noise. They allow the signal transfer from the bottom to the top. Noise from the top is absorbed by the terminated third in/output on the side of the circulator. A signal passing the circulators is amplified by a HEM (high electron mobility) cold low noise amplifier (further described in Section 6.3). The following attenuator is used to attenuate reflections arriving from the top.

DC voltage sources are used at room temperature in combination with a resistive low pass filter to implement a DC current source. The electric current is sent through the superconducting coils that generate a constant flux which tunes the qubits transition frequency ω_a.

The microwave pulse generation mainly makes use of microwave sources, arbitrary waveform generators (AWG) and I-Q-mixers, compare Figure 3.3. In fact only one AWG is used which provides four different waveform channels and eight markers. All of these are arbitrary programmable with a sampling rate of 1 GHz. A trigger source (not shown in Figure 3.3) triggers the AWG which itself distributes trigger over the programmable markers to the data acquisition cards in the signal analysis and to the other instruments in the microwave pulse generation. The microwave sources (generating coherent microwaves with desired power and frequency) can be switched on and off ("mod") by the markers of the AWG. In this way a pulsed measurement is implemented. The "RF" microwave source is switched off after the AWG received a trigger. After further 5 μs the "RF" is switched on to generate the measurement signal that is transferred directly into the refrigerator to the input of the resonator.

To generate the control pulses for the qubits the generators "Spec" and "Stark" are used. Because the qubit pulses are very short ($\sim$ 10 ns) the switching on and off results in poor control pulses. Therefore, I-Q-mixer are used to perform the switching. An ideal I-Q-mixer splits up the "LO" input into two, one of them phase shifted by $\pi/2$. The two parts are multiplied with the signal at the input "I" and "Q" respectively. Then the two multiplied signals are combined without phase shift (Schmidlin, 2009) to the "RF" output of the I-Q-mixer. Using this characteristic of the I-Q-mixer it is possible to let the signal entering the "LO" input pass through the mixer ($I = 1$ and $Q = 0$) or to block the signal ($I = 0$ and $Q = 0$) or to let the signal pass with a $\pi/2$ phase shift ($I = 0$ and $Q = 1$). The configuration of I and Q can be controlled by the markers of the AWG. To prevent leakage through the mixer a backup pulse is sent to the microwave generator to switch the output on only around the time the mixer allows the signal pass.

Unfortunately, the applied phase shift of the I-Q-mixer is not exactly $\pi/2$, the multiplica-

tion processes are not equal and there are offsets leading to leakage through the mixer. To obtain better shaped qubit control pulses the I-Q-mixer are used as downconverter. A shaped sine and cosine with intermediate frequency 100 MHz are generated with two channels of the AWG and fed to the I and Q inputs of the mixer. When the mixer is calibrated appropriately only one sideband of the "LO" input (frequency ν_{LO}) is generated with a well defined phase shift and frequency $\nu_{\mathrm{LO}} - 100\,\mathrm{MHz}$. The calibration is necessary for every desired ν_{LO} separately by manually searching for two offsets, which are applied on the I and Q inputs, and for a phase offset and an amplitude to scale the cosine to the Q input. For details of the calibration procedure see Schmidlin (2009). The three above described pulse generations (microwave pulse generation, I-Q-mixer switching and calibrated I-Q-mixer switching) are interchangeable and all of them were used in my experiments.

The amplifier following the "Stark" line is used to implement pulses strong enough for two photon transitions. Further there are attenuators between mixers, amplifier and splitter (big dots, combining two signals) to avoid not desired pulses due to reflections.

The transmission signal analysis (compare Figure 3.3) is described from bottom to top, as this is the direction the signal passes. A signal with frequency $\nu_{\mathrm{meas}} \sim 6.5\,\mathrm{GHz}$ and noise leaving the cryostat are amplified. It follows an attenuator (not displayed) to avoid possible reflections and a bandpass filter which allows the pass of frequencies from 5.5 GHz to 8 GHz to limit noise power being able to saturate the consecutive amplifier. Then the signal is mixed by an I-Q-mixer used as a downconverter. In contrast to the mixer applied in the pulse generation the "RF" is used as an input and I and Q are used as outputs. The "RF" input is split up into two equal parts. A microwave with frequency $\nu_{\mathrm{meas}} + \nu_{\mathrm{if}}$ with ν_{if} typically 10 MHz or 25 MHz is generated and fed into the "LO" input where it is split up into two parts, one of them phase shifted about $\pi/2$. In the mixer there are now two times two signals which are multiplied together, one "RF" term with one "LO" term, and passed to the outputs I and Q respectively. The output $I(t)$ has the form

$$\begin{aligned} I(t) &= A_{\mathrm{RF}} \sin(2\pi\nu_{\mathrm{meas}} t) \cdot A_{\mathrm{LO}} \sin(2\pi(\nu_{\mathrm{meas}} + \nu_{\mathrm{if}})t) \\ &= \tfrac{1}{2}\, A_{\mathrm{RF}}\, A_{\mathrm{LO}}\, \left[\cos(2\pi\nu_{\mathrm{if}} t) - \cos(2\pi\,(2\nu_{\mathrm{meas}} + \nu_{\mathrm{if}})\,t)\right], \end{aligned}$$

where A_{RF} and A_{LO} are the amplitudes of the signal at input "RF" and "LO" respectively. The output $Q(t)$ is just shifted by $\pi/2$. It is obvious that the output signal consists of a term oscillating with frequency ν_{if} and a very fast oscillating term with frequency $2\nu_{\mathrm{meas}} + \nu_{\mathrm{if}}$. This mixing process is also referred to as analog downconverting. The two very similar (just phase shifted) outputs I and Q from the mixer are amplified a last time and the fast oscillating term $2\nu_{\mathrm{meas}} + \nu_{\mathrm{if}}$ is filtered out completely by a consecutive low pass filter. A second task of this low pass filter is to prevent the following analog to digital converter (ADC) from aliasing, further dealt with in Section 5.2. The filter is therefore also referred to as anti-aliasing filter. In this work all experiments are performed with a 30 MHz low pass filter (Mini-Circuits, n.d.). After the two signals passed the anti-aliasing filter they are digitised with an ADC of sample rate 1 GHz on a data acquisition card by Acqiris (used to average the data) and with an ADC of sample rate 100 MHz on the FPGA card

(used to perform single shot analysis).

All the microwave sources, AWGs, triggers and data acquisition cards are phase locked with an external rubidium 10 MHz reference clock. This is crucial to avoid the accumulation of phase differences during long measurements. Otherwise downconverting the signal with a fixed phase, which is important when averaging a quadrature signal, would be impossible. For later single shot analyses it is also important to have the signal at a fixed phase in the I-Q-plane and not slowly rotating in the same. A well defined phase is also important for phase stable qubit control pulses.

With the measurement setup described above it is possible to perform time resolved transmission measurements further described below in Section 3.3 by implementing the desired qubit control and measurement pulse sequences into the AWG and setting up the microwave sources appropriately in the pulse generation section of Figure 3.3. Not time resolved measurements are also possible. To determine the cavity resonance frequency a frequency sweep of the "RF" microwave source is performed and the averaged transmitted homodyne amplitude for each "RF" frequency is analysed. An amplitude A is calculated from the homodyne quadrature signal $I+i\,Q$ to $A = \sqrt{I^2 + Q^2}$ and the phase is calculated to $\arg(I + i\,Q) = \pm \arctan(Q/I)$. The maximum amplitude is observed when the "RF" frequency match the cavity resonance frequency as there is no signal reflected by the resonator. Spectroscopic measurements are performed by the "Spec" microwave sources either through the gate lines or even through the resonator line. In addition the "RF" microwave source is irradiating microwaves with the resonance frequency of the cavity. A frequency sweep of the "Spec" generator is performed and the averaged transmitted homodyne "RF" amplitude is analysed. In the case in which the frequency of the "Spec" source matches a transition frequency of the transmon, the transmon performs incoherent Rabi oscillations. Average shifts of the cavity resonance frequency results in a dip of the transmitted "RF" amplitude. Qubit selected spectroscopy is performed using the "Spec" microwave source attached to the specific gate line.

3.3 Measurement signal analysis

Unfortunately, the measurement signal is dominated by noise which is mainly added by the first cold amplifier in the measurement setup (compare Figure 3.3). The quadrature signal $I(t)+i\,Q(t)$ (presented in Section 2.3) is averaged over a number of shots J, as later described in Section 4.4.3, to reduce the noise amplitude by $\sqrt{1/J}$, compare Section 5.3.1. In the following a single qubit preparation together with the subsequent measurement pulse is called "a shot". The drawback of averaging over a number of shots is that different decay times of the qubit are together averaged. The decay time of a qubit is spontaneous. It is assumed that the decay time T_d from state $|e\rangle$ to $|g\rangle$ is exponentially distributed. Similarly to the radioactive decay of atoms a characteristic decay time for T_1 is in the order of 1 μs. Note that T_d cannot be predicted. Averaging only shots with a definite qubit decay time is therefore impossible. From state $|g\rangle$ to $|e\rangle$ there is no decay and therefore the averaged measurement response corresponds to the single shot

measurement response.

From the averaged measurement response we want to infer the single shot measurement response. The most complete model for the averaged measurement response takes energy relaxation and dephasing for the dispersive limit in circuit QED (see Section 2.3) into account. This model is described by the cavity Bloch equations presented by Bianchetti et al. (2009). In addition, a pulsed measurement is considered here, so that a cavity with resonance frequency ω_r is populated at rate κ when a driving field with frequency ω_{meas} is switched on suddenly. The population of the cavity follows as

$$\langle a(t) \rangle = -\epsilon \frac{1 - e^{-\frac{\kappa}{2}t - i(\omega_{\text{meas}} - \omega_r)t}}{(\omega_{\text{meas}} - \omega_r) - i\,\kappa/2},$$

where κ is the cavity decay rate and ϵ the driving amplitude. (Bianchetti et al., 2009; Walls and Milburn, 2008). As can be seen easily, populating the cavity off resonant results in a damped ringing with frequency $\omega_{\text{meas}} - \omega_r$ until the new steady stated is reached. For the excited state $|e\rangle$-response it is additionally necessary to take qubit energy relaxation into account. The resulting cavity Bloch equations are eight differential equations, obtained by a master equation approach, which are solved numerically to fit the averaged measurement response.

Experimentally the qubit is prepared in the ground state $|g\rangle$ and the measurement response for different measurement frequencies ω_{meas} around ω_r' (compare Section 2.3) are averaged for a pulsed measurement. Analogously the qubit is prepared in the excited state $|e\rangle$ just before the measurement pulse is switched on. The experimental data is shown in Figure 3.4 by blue (for state $|g\rangle$) and red (for state $|e\rangle$) dots. Green dots indicate the difference between excited and ground state and are shown because information about the qubit state is gained by the difference of the two measurement responses. To achieve a better fit to the cavity Bloch equations the measurement responses for the different ω_{meas} are used. The numerical solution of the cavity Bloch equations for the averaged responses is shown by the lines in Figure 3.4. The ground state response does not show strong oscillations caused by the abrupt cavity population as the measurement frequency ω_{meas} and cavity resonance frequency $\omega_r' - \chi$ (compare Section 2.3) are very similar. Around 500 ns comparable to $1/\kappa$ the measurement response has reached its steady state amplitude. The excited state measurement response shows the characteristic oscillations of the abrupt cavity load. The nonzero signal at $-5\,\mu$s in Figure 3.4 is caused by switching off the measurement signal at this time to give the qubit enough time to relax into state $|g\rangle$.

Once the parameters are obtained the measurement response for a qubit with specific decay time T_d or even a non decaying qubit can be calculated as shown in Figure 3.5. The calculation of the theoretical measurement response for the two states $|g\rangle$ and $|e\rangle$ with a specified decay time T_d is important as these responses correspond to the single shot signal without noise. In subsequent sections of this work we will need the single shot signal measurement response to perform single shot measurement analyses.

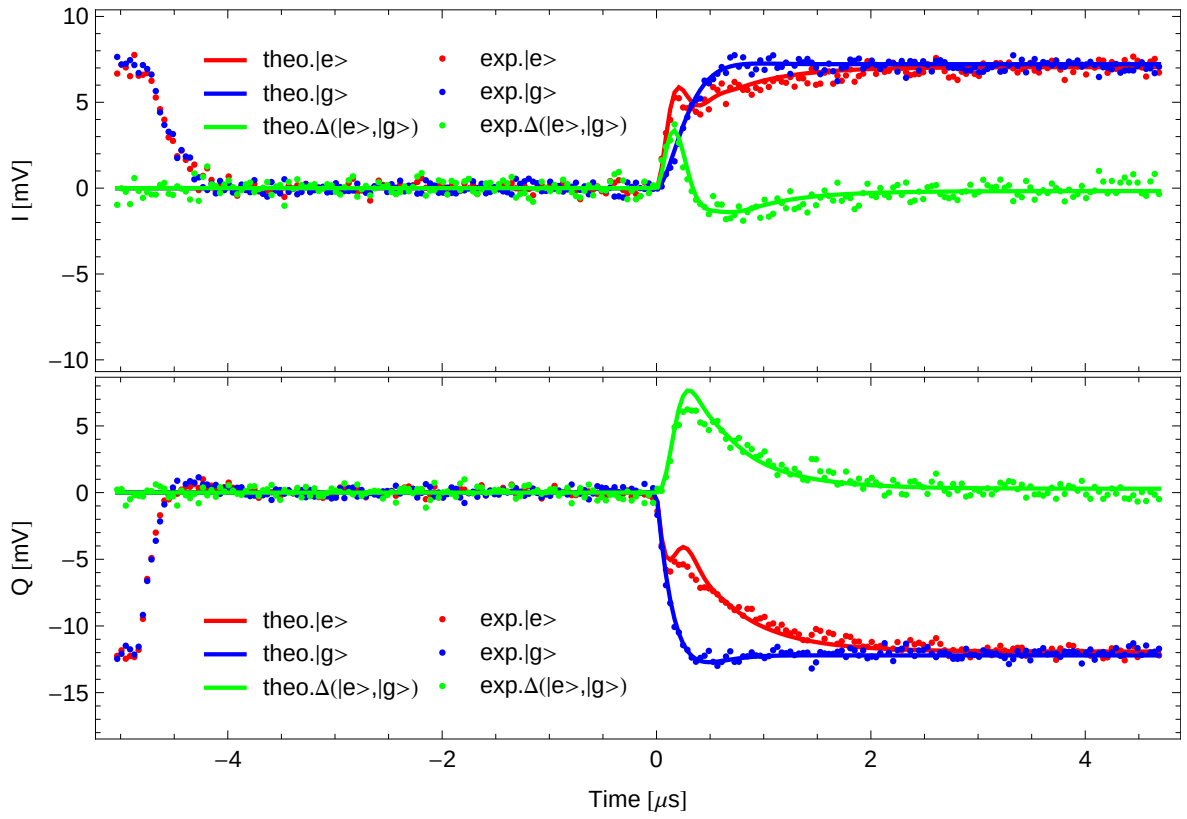


Figure 3.4: Experimental averaged pulsed measurement response (dots) for the homodyne quadratures $I(t)$ (top) and $Q(t)$ (bottom). Lines represent the numerical solution of the cavity Bloch equations with parameters $\nu_r' = 6.44513\,\mathrm{GHz}$, $\kappa = 1.725\,\mathrm{MHz}$, $\chi = -0.96\,\mathrm{MHz}$ and $T_1 = 520\,\mathrm{ns}$ at a measurement power of $-19\,\mathrm{dBm}$ ($\langle n \rangle \approx 10$). Here the measurement response is shown for the measurement frequency $\nu_{\mathrm{meas}} = 6.44564\,\mathrm{GHz}$. The difference between excited state (red) and ground state (blue) response is shown in green.

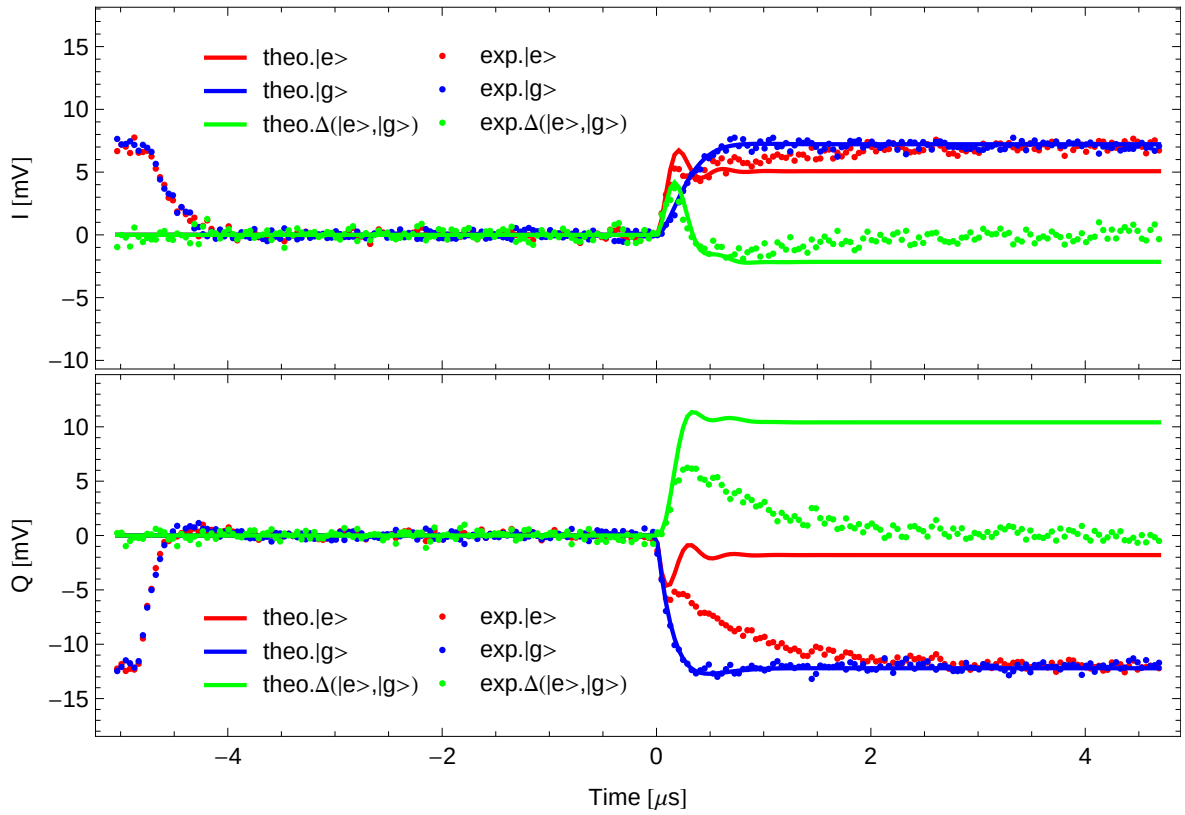


Figure 3.5: Same quantities as shown in Figure 3.4, but with qubit relaxation time chosen to be $T_1 = \infty$. The theoretical cavity Bloch measurement response is equal to the single shot measurement response which we expect for the case in which the qubit lives longer than 5 μs during the measurement. Here the oscillations are purely caused by off resonant population of the cavity.

Chapter 4

Field programmable gate array (FPGA) card

In the previous chapter the measurement setup was introduced. In this setup I integrated a FPGA card to perform real-time measurement signal analysis, in particular single shot read-out of qubit states. In this chapter the FPGA card and its integration in the setup will be described. The first section shortly explains a FPGA. Afterwards the hardware of the FPGA card is described. In Section 4.3 the implementation of the controlling of the FPGA is presented. Section 4.4 introduces the applications that run on the FPGA and their purpose. In the last section the software, that controls the FPGA and the measurements performed on the FPGA, and its use is introduced.

4.1 FPGA description

A field programmable gate array (FPGA) is a programmable digital integrated circuit (Kaeslin, 2008). It is a chip on which digital hardware can be "programmed" on. The main components a FPGA consists of are programmable logic blocks, divided into a small lookup table (LUT) and a clocked flip flop. These logic blocks are used as configurable logic gates such as AND, NOT, NOR, etc. In addition to the programming of the LUTs the logic blocks can be programmatically connected and combined in the gate array (Kaeslin, 2008), so that the simple logic gates combined can perform more complex digital functions. Simple digital tasks, such as a counter or encoder as well as more complex circuits, e.g. one or more processors or even a microcontroller, can be programmed. The clock is set in the FPGA and needs not to be the same for different logic blocks. Often FPGAs include additional higher integrated blocks, which are more specific but faster as if they would be implemented only using combined logic blocks. Such higher integrated blocks are e.g. multiplier or input and output blocks to communicate with the outside (Kaeslin, 2008). Blocks that cannot be reproduced by the logic blocks are memory blocks, in the most simple case a flip flop, or even a block random access memory (RAM). They are therefore already integrated into the FPGA.

Once the design is implemented on the FPGA it can be regarded as a highly integrated digital circuit performing the task intended for. As in a hardware wired circuit all logical

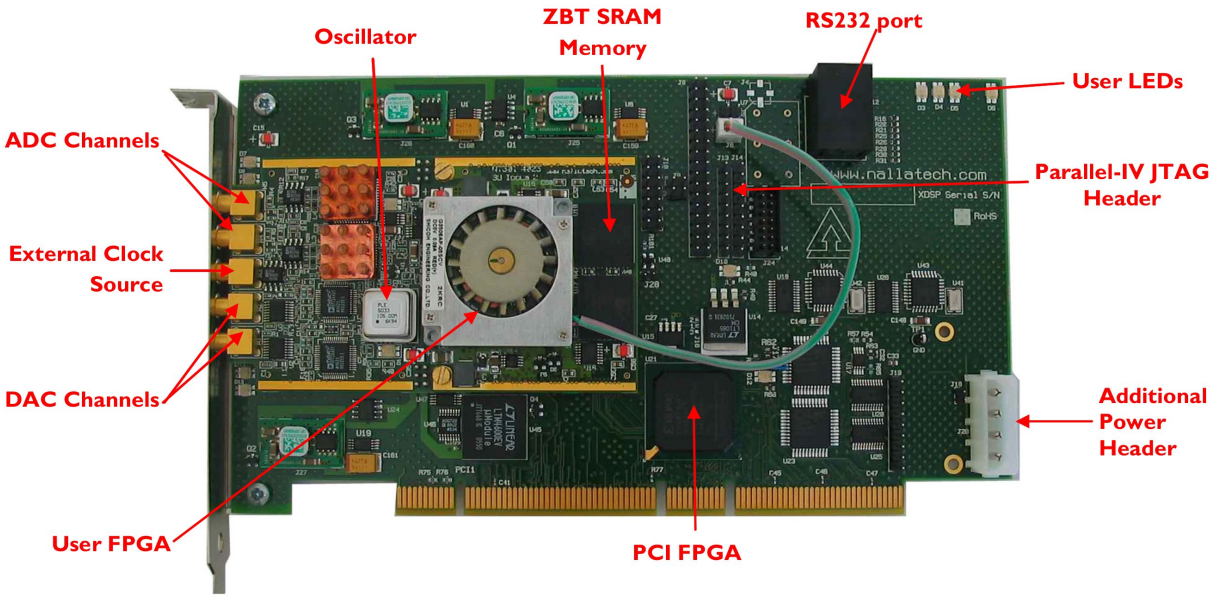


Figure 4.1: Photo of the FPGA card with labels on the most important components (Nallatech and Xilinx, 2007a).

gates in the circuit are evaluated in parallel and "instantaneously" (this is completely different to a processor which perform logical operations, one in each clock cycle, sequentially) only giving raise to timing problems when the logical paths become too long. To solve these timing problems some critical operations can be clocked. Nevertheless, these operations are performed all in parallel but executed in a pipe-like manner. For example the multiplication is divided into two steps where each step is handled by logical gates. The first pair of factors enters the multiplicator and step one is performed during the first clock cycle. In the second clock cycle the second pair of factors enters step one while on the first pair step two is performed and the product of the first pair leaves the multiplicator. During the next clock cycle a third pair can enter while the second product is finished, and so on. This parallel and pipe like behaviour in the FPGA is a fundamental difference to a processor and builds the basis for the power of the FPGA performing specific tasks (within a fixed time) much faster than regular processors could do.

4.2 Hardware

The hardware used in the context of this thesis is the "XtremeDSP Development Kit-IV" built by Nallatech with three FPGAs from Xilinx (Nallatech and Xilinx, 2007b). This Xilinx distribution should support the sale of their FPGAs and software to program the FPGAs. The FPGA card, on which the FPGAs are mounted, mainly consists of two components, a "BenONE PCI" motherboard and a "BenADDA" module installed on the motherboard (Nallatech, 2006a). Both are distributed with additional electronic components that can be used by the FPGAs. See Figure 4.1 for a picture of the FPGA

card (Nallatech and Xilinx, 2007a) with the most important components labelled.

The components of the "BenONE PCI" motherboard, that are of main interest for us, are the PCI interface, the "PCI FPGA", the "Parallel-IV JTAG Header" and the connection to input and output blocks on the "User FPGA", compare Figure 4.1. On the "PCI FPGA" runs a fixed program enabling the communication between the PC and the "BenONE PCI" motherboard through the PCI interface. For example, the programming of the two FPGAs on the "BenADDA" module is done using this connection. Further we connected four pins on the "Parallel-IV JTAG Header" to BNC connectors on the back of the PC, referred to as "UserPin" zero to three. Each of them provides a direct bi-directional digital connection to input and output blocks on the "User FPGA" (Nallatech and Xilinx, 2007b). They are used as triggers in the current setup.

The "BenADDA" module is packed with further important components (see Figure 4.1). An external 10 MHz reference clock, to which all the other instruments in the experiment are locked to, is connected to the "External Clock Source". The "External Clock Source" is connected to the "Clock FPGA" which is able to distribute a further modified clock to all the other digital components. The external clock is crucial as even a slight drift between the analog to digital converters (ADC) on the FPGA card and the measurement signal phase is imperative to be avoided. The main component on the "BenADDA" is the "user FPGA" a Virtex 4 FPGA XC4VSX35-10FF668 (Nallatech and Xilinx, 2007b). The "user FPGA" is connected via input and output blocks to the motherboard and the other components on the "BenADDA". There are further two independent banks of "ZBT SRAM Memory" each featured with 512K x 32 bit resulting in two times 2 Mb. Two independent ADCs and two independent digital to analog converter (DAC), all capable for external clocking, are connected additionally to the "user FPGA". The ADCs have a full range of ± 1.1 V with a resolution of 14 bit and a sample rate up to 105 MHz, fast enough to sample both quadratures of a 25 MHz signal. The DACs also have a resolution of 14 bit but with a sample rate up to 160 MHz and a full range of ± 1 V. The FPGA card is very suitable for our needs due to the additional electronic components, such as the appropriately dimensioned ADCs, the external clock input, the RAM and the PCI interface.

4.3 Controlling

Figure 4.2 shows the implementation scheme that is programmed on the FPGA card providing us the necessary functions described in the following. There are two programmable FPGAs on the card. The first one is the "clock FPGA". By means of VHDL (VHSIC (very high speed integrated circuit) hardware description language) a 100 MHz clock phase locked to the external 10 MHz reference clock is implemented. This 100 MHz clock is then distributed to the user FPGA and the other digital components on the "BenADDA" namely the ADCs, DACs, RAMs, compare Figure 4.2. The "UserPins" are sampled at the newly generated clock as the "user FPGA" is clocked with it. The VHDL code is compiled by the Xilinx ISE Studio into a ".bit" file that can be loaded into the "clock

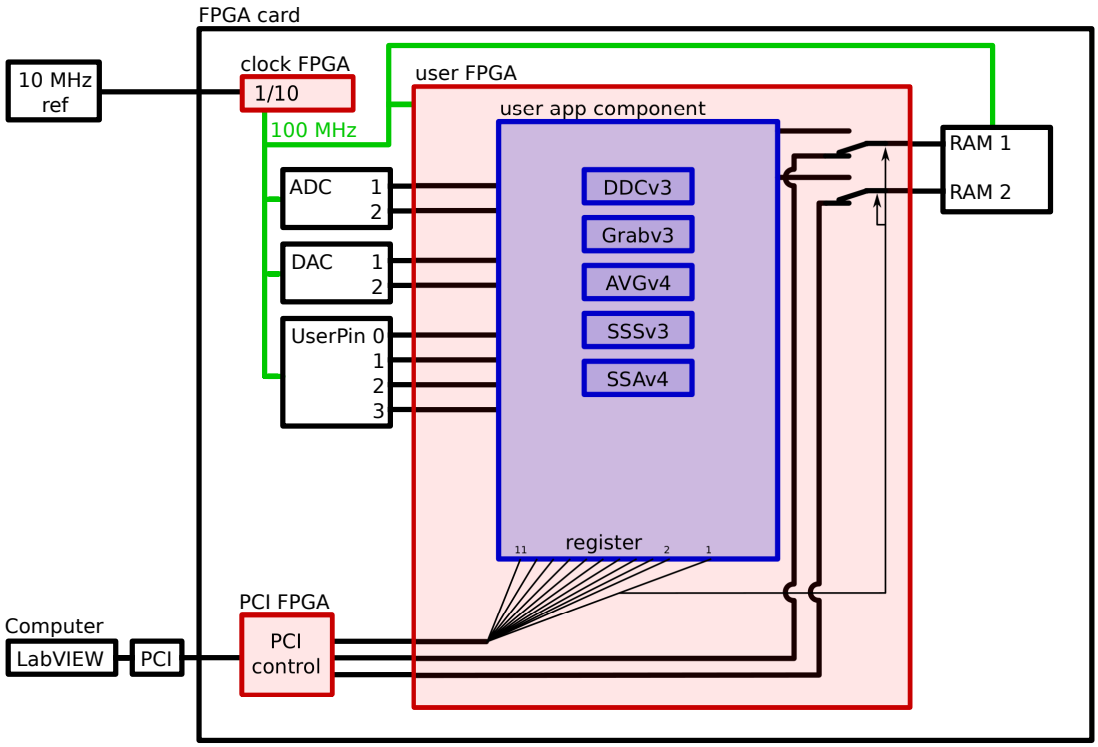


Figure 4.2: Sketch of the FPGA controlling. The clock distribution (green) and the three FPGAs (red) on the card are shown. The applications (blue) in the "user app component" are described in Section 4.4

FPGA". The generation of the 100 MHz clock using an external clock ensures that the external reference clock is plugged before programming the "clock FPGA". In the case of a loss of the reference clock, for example after a PC restart, the generated 100 MHz clock shuts down until the "clock FPGA" is reprogrammed. After the programming of the "clock FPGA" all components on the "BenADDA" are clocked with 100 MHz locked to the external reference clock. Henceforth the clock is referred to as sample frequency $f_s = 100\,\text{MHz}$ because the ADCs and DACs are clocked with this clock frequency and all the other components synchronous to it.

The "user FPGA" needs to fulfil more functions simultaneously. As the reprogramming process lasts in the order of seconds it is not sufficient to have different programs for different tasks such as one program for measuring and one for reading out of the RAM. The "user FPGA" needs to provide an interface to the PC via the "PCI FPGA" and to be capable to store analysed data in the RAMs to be read out afterwards by the PC. With the FPGA card there was delivered some example code, amongst others VHDL code that interfaces one bank of RAM to the "PCI FPGA" providing five 32 bit wide internal registers, controlling the read and write processes and transferring data from and to the PC. This example code was extended to interface both banks of RAM. Further eleven more bidirectional registers, referred to as register one to eleven, were introduced. They act as variables able to share $11 \times 32\,\text{bit}$ of information between PC and FPGA.

These registers can be read and written by using the FUSE development API for C/C++ (Nallatech, 2006b) delivered with the FPGA card. It works similarly to the control of the read and write processes of the RAM. More example code was integrated into the program to provide interfaces that handle the other components on the FPGA card such as the ADCs, the DACs, some LEDs, the "UserPins" and a conventional interface to let the "user FPGA" make use of the RAM. Bit 0 and bit 1 of register one are used to switch between the conventional interface and the interface connected to the "PCI FPGA" for each bank of RAM individually. So we end up with VHDL code producing the functionality sketched on the red shaded area of the "user FPGA" in Figure 4.2.

In the VHDL code, that provides an interface to all the components including the external PC and establishes a RAM switch, the "user app component" is embedded (see Figure 4.2). The "user app component" is designed to integrate the applications for signal processing and signal analysis. The data lines from the ADCs are wired to the "user app component". Analogously data lines from the "user app component" are wired to the DACs and to the conventional RAM interface. Since the API, the "user app component" will be integrated in, does not support bidirectional wires register one to ten are connected to the "user app component" in a way that warrants that the "user app component" can read them. Register eleven is connected to the "user app component" so that this register can be written by the "user app component". The same applies for the "UserPins" whereby all four are connected readable. The VHDL code described in the previous paragraphs is referred to as "wrapper" because it wraps around the "user app component". As the "wrapper" provides all the features of the FPGA card to the "user app component" it does not need to be changed any more even in the case applications in the "user app component" are changed or added.

The "user app component" is programmed in the Matlab extension Simulink (for which Xilinx provides an extension to graphically design "FPGA code"), which later can be compiled into VHDL code. An example of this graphically designed code is shown in Figure 4.3. The example makes use of various logical operations, mathematical functions, etc., available in the Simulink library implementing a digital downconversion further described in Section 4.4.1. Here, basic elements are for example: "Mux": switching instantaneously between the channels "d0", "d1", etc. in dependence of the input "sel". "Delay": passing the input in a pipe-like manner with a delay of some clock cycles. "Add-Sub", "Mult", "ConstMult": performing mathematical functions in fixed point arithmetic. "Accumulator": accumulating its clocked input while enabled. "DDS Compiler": synthesising sinusoids with desired frequency and phase offset. "positive edge": returning a one when detecting a positive edge. It consists of basic elements such as a delay line, an inverter and a logical AND. The wires connect all the blocks in the desired manner that the intended task is performed. Codes, similar to the example, implementing more applications and making use of ADCs, DACs, "UserPins" and RAM are connected appropriately and form the "user app component". There are eleven registers connected to the "user app component" (see Figure 4.2) each of width 32 bit. Register one to ten can only be written by the PC. Register eleven is set by the FPGA. However, both the FPGA and the PC are capable to read all these registers, so that the last register eleven is used to get feedback

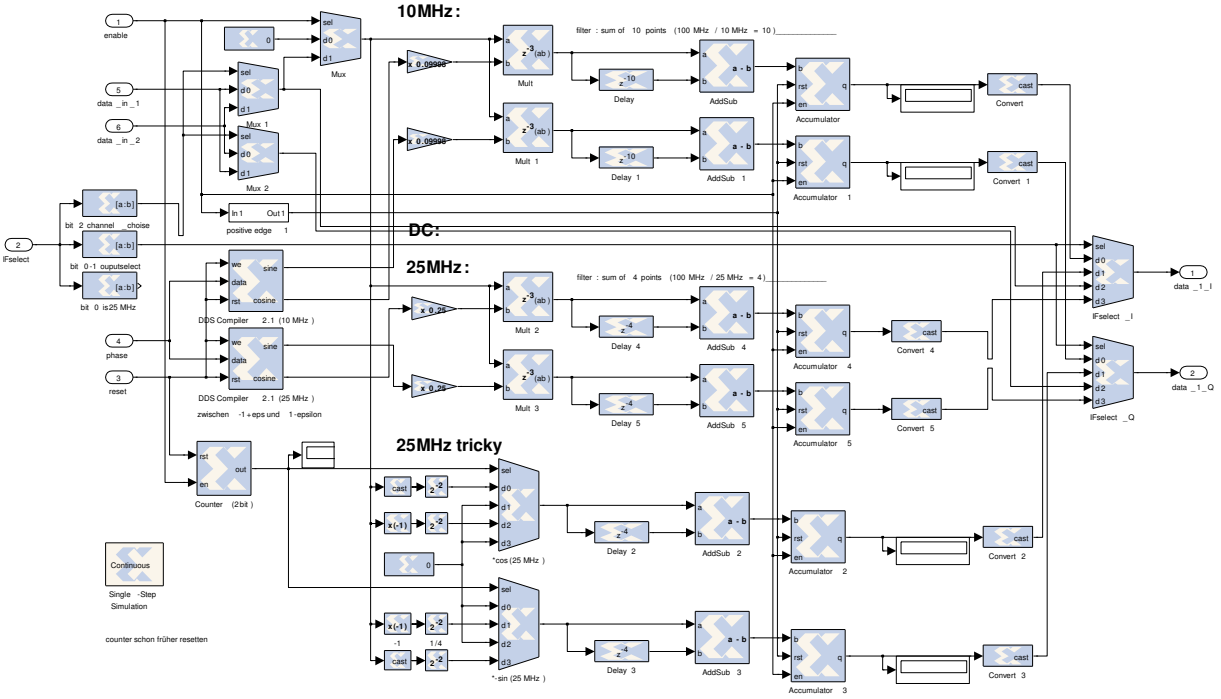


Figure 4.3: DDCv3 (see Section 4.4.1) graphically designed in Simulink. All besides the positive edge detector are basic components provided by the Simulink library of Xilinx. The wires connect all the blocks in the desired manner that the incoming 14 bit fixed point data are downconverted as described in Section 4.4.1. The data in this example is mainly flowing from left to the right in a branching pipe.

from the FPGA. This register contains the status of the various applications implemented in the FPGA. The status indicates whether an application has finished or is still running. A second very important register is register one, which is used to start, stop or reset some set of the applications running on the FPGA. Bits 2 to 4 tell the "user app component" which application (1 to 7) should be started writing its data to RAM bank one. Thereby number 0 does not start any application. Similarly bits 5 to 7 of register one start the specified application with access to RAM bank two. The applications are programmed to reset and start when a raising edge on their application number is detected. In addition bit 0 and 1 need to be set appropriately as they switch the control over the specific bank of RAM to the "user app component". Neither the PC nor other applications running on the FPGA can then read or write to that bank of RAM. To give the control over the RAM back to the PC the application is stopped by changing the register one back to zero, ideally when the application has finished (indicated by register eleven). The remaining registers, two to ten, are used to setup the applications and to pass parameters. In Section 4.4 the applications running in the "user app component" are described. When the "user app component" is programmed in the desired manner it can be compiled into VHDL code. Together with the "wrapper" VHDL code it is compiled by the Xilinx ISE Studio into a ".bit" file that can be loaded into the "user FPGA".

Throughout the course of this work an additional library was written in the programming

language C to provide functions to communicate with the FPGA. These functions make use of the FUSE development API for C/C++ to communicate with the motherboard of the FPGA card over the DIME-II standard (see Chapter 2 of Nallatech and Xilinx (2007b) for details). Amongst others the functions are able to (re-)program the "clock FPGA" and "user FPGA", to read and write data from or to the two banks of RAM and to read and write register one to eleven. Section 4.5 describes the functions available in the library to control the FPGA.

4.4 Applications

In this section the applications which I programmed into the "user app component" are described. A block diagram is shown in Figure 4.4 intended to give an overview of the overall structure of the programs that run on the FPGA. From the block diagram it arises how the applications, described in the following sections, are wired to the hardware, and how they are started (with register one), parameterised with (with register two to ten) and give feedback on their running status over register eleven. The application numbers (specified by the bits) are assigned in the order the application blocks are wired from "app $0x$ enable" ($x = 1, \ldots, 7$) of the "Decoder_01" to the "enable" input of the corresponding application block. The switching of the RAM banks assigned to the started applications as described in Section 4.3 is performed in the "ZBT RAM" block in dependence of the "zbtCtrl" input. In the following five sections the programs of the "user app component", their functionality and how they are set up correctly, are described.

4.4.1 Digital Downconverter v03

The Digital Downconverter v03 (DDCv3) is used to convert a heterodyne signal $x(t_n)$ with intermediate frequency (IF) ν_{if} sampled by the ADCs into a homodyne quadrature signal $I(t_n) + i\,Q(t_n)$. A block diagram of the DDCv3 implementation is shown in Figure 4.3.

The measurement signal that leaves the circuit QED system has a typical frequency of $\approx 6.5\,\text{GHz}$. Such a fast oscillating signal is very hard to digitise (and ADCs for this purpose are also very expensive). Therefore it is analogically downconverted to an IF $\nu_{\text{if}} = 10\,\text{MHz}$ or $\nu_{\text{if}} = 25\,\text{MHz}$ as described in Section 3.2. These frequencies are slow enough that the measurement signal can be digitised (with sample frequency $f_s = 100\,\text{MHz}$) and processed appropriately to extract both quadratures of the signal with time resolution of $1/\nu_{\text{if}}$ (due to Nyquist theorem the highest possible IF to extract both quadratures of a digitised real signal is $\nu_{\text{if}} = f_s/4 = 25\,\text{MHz}$). This application homodynes the digitised signal from ν_{if} to DC. Since most other applications need a homodyne signal for an appropriate signal analysis the DDCv3 is an essential signal processing block running on the FPGA.

It is an usual method to digitise a heterodyne signal that is digitally homodyned rather than a homodyne signal. Digitising a homodyne signal would need two very accurate

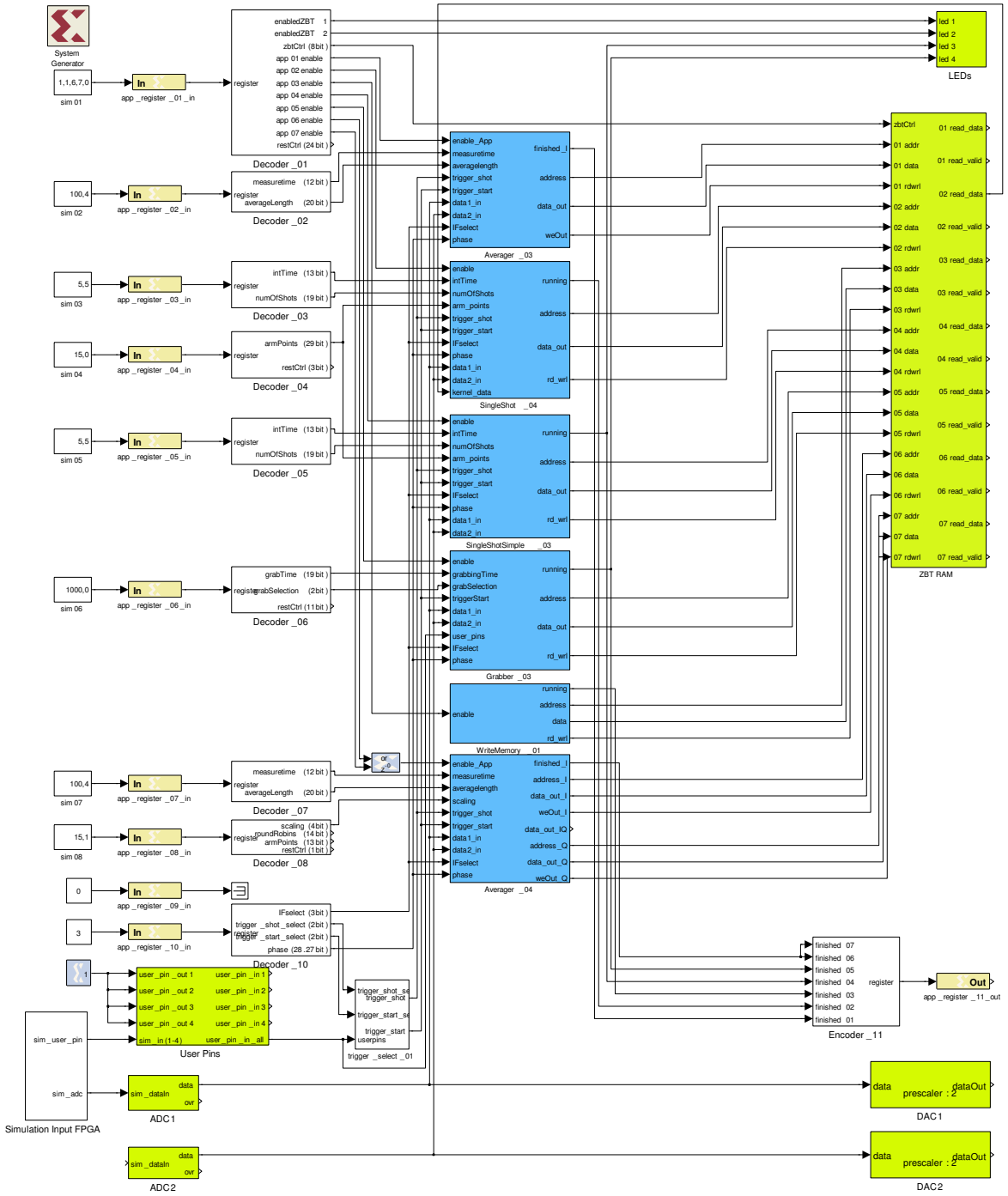


Figure 4.4: Block diagram of the "user app component". It provides an overview of the programs that run on the FPGA. The blue blocks represent the applications and the green blocks are connected to the hardware installed on the FPGA card. The registers, read and set by the PC over the PCI interface, are marked in beige and are decoded and encoded by the white blocks respectively. The other smaller white blocks serve as simulation inputs for the "user app component". The wires connect the blocks appropriately.

balanced ADCs with no parasitic DC offsets. This problem is avoided with a heterodyne signal which only needs one ADC. Any parasitic DC offset is here filtered out automatically, as described below. The cost of this method is a reduced time resolution of $1/\nu_{\text{if}}$ instead of the sample frequency f_s (Lyons, 2004).

Parameters

There are several DDCv3 in the design of the FPGA, in most applications (Section 4.4.2, 4.4.3 and 4.4.4) one is embedded. All receive its input by two analog to digital converters (ADC1 and ADC2). Register ten sets up the DDCv3.

Bits 0 to 1 signalise the DDCv3 which IF out of four different possibilities should be used. Two of them perform standard digital downconversion: $\text{IF}_{00} = 10\,\text{MHz}$ and $\text{IF}_{11} = 25\,\text{MHz}$. In these two settings a phase offset for the digital downconversion can be set in bit 7 to 31 which is applied on reset of the DDCv3. When IF is set to $\text{IF}_{01} = 25\,\text{MHz}$ a quicker downconversion method is performed with no need of multiplications in the FPGA, furthermore referred to as "tricky" downconversion. When the input signal is homodyne yet one selects $\text{IF}_{10} = 0\,\text{Hz}$ so that the output of the DDCv3 is not downconverted with $I = \text{ADC1}$ and $Q = \text{ADC2}$.

Bit 2 of register ten selects the ADC to use for downconversion where 0 denotes ADC1 and 1 denotes ADC2. In the case IF is selected to IF_{10} 0 denotes $I = \text{ADC1}$ and $Q = \text{ADC2}$ and 1 swaps I and Q to $I = \text{ADC2}$ and $Q = \text{ADC1}$.

There are four digital inputs to the FPGA called "UserPins" 0 to 3 which serve as trigger of the measurements. It is intended to deliver two triggers to the FPGA card. The raising edge of one, referred to as the shot trigger, announces the start of each single experiment (shot). The raising edge of the other, referred to as the start trigger, announces the start shot when different qubit states are prepared consecutively. In which of the "UserPins" 0 to 3 the shot trigger and the start trigger are plugged is chosen by bits 3 to 4 and bits 5 to 6 respectively.

Concept

The DDCv3 implements the most simple digital downconversion method, further details and more complex methods are described in Lyons (2004).

Real valued digitised data $x_{\text{dig}}(t_n)$ taken at the discrete time points t_n, $n = 1, \ldots, \infty$ enter the DDCv3. If $\text{IF} \neq 0\,\text{Hz}$ the data is multiplied with a complex sinusoid with frequency ν_{if} equal to the selected IF:

$$\begin{aligned} x_{\text{downc}}(t_n) &= x_{\text{dig}}(t_n) \cdot [\cos(2\pi\nu_{\text{if}} t_n + \varphi) - i \sin(2\pi\nu_{\text{if}} t_n + \varphi)] \\ &= x_{\text{dig}}(t_n) \cdot e^{-i\,2\pi\nu_{\text{if}} t_n + \varphi} \\ &:= I_{\text{downc}}(t_n) + i\, Q_{\text{downc}}(t_n), \end{aligned} \tag{4.1}$$

where an arbitrary global phase offset φ can be chosen. However, the only effect is a

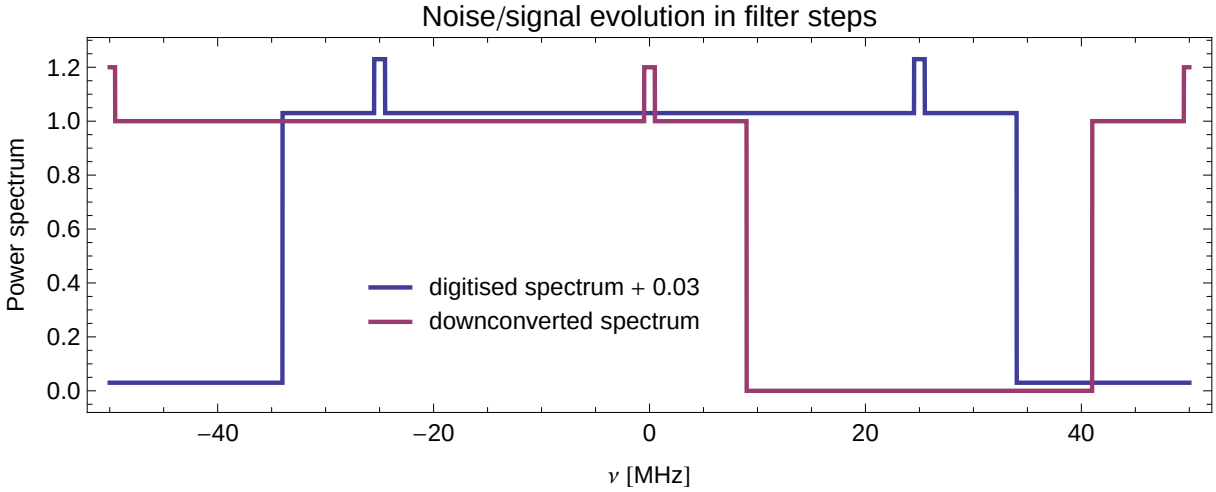


Figure 4.5: Sketch of power spectrum for data digitised by one of the ADCs (digitised spectrum). After multiplication with 25 MHz sinusoids the spectrum is shifted by 25 MHz to the left (downconverted spectrum). Spectral content disappearing on the left reappears on the right side.

rotation by φ of the downconverted quadrature signal in the I-Q-plane. In this operation the spectrum of $x_{\mathrm{dig}}(t_n)$ is shifted down by ν_{if} as shown in Figure 4.5. A signal of $x_{\mathrm{dig}}(t_n) = \cos(2\pi f t_n)$ has a Fourier spectrum $X_{\mathrm{dig}}(\nu)$ with two nonzero Dirac delta bins $\delta[\nu]$ at $\pm f$:

$$X_{\mathrm{dig}}(\nu) = \tfrac{1}{2} \cdot \delta[f - \nu] + \tfrac{1}{2} \cdot \delta[f + \nu].$$

After the multiplication with $e^{-i\,2\pi\nu_{\mathrm{if}}t_n}$ the bins in the Fourier spectrum $X_{\mathrm{downc}}(\nu)$ are shifted to a lower frequency by the amount of ν_{if}:

$$X_{\mathrm{downc}}(\nu) = \tfrac{1}{2} \cdot \delta[(f - \nu_{\mathrm{if}}) - \nu] + \tfrac{1}{2} \cdot \delta[(f - \nu_{\mathrm{if}}) + \nu],$$

where the nonzero bins are located at $\pm f - \nu_{\mathrm{if}}$. As $x_{\mathrm{dig}}(t_n)$ is a real signal the Fourier spectrum is symmetric around zero frequency. After the downconversion step the signal $x_{\mathrm{downc}}(t_n)$ is not real any more (compare Equation 4.1) and therefore its spectrum (Fourier transform of $x_{\mathrm{downc}}(t_n)$) is no longer symmetric around the zero frequency (Lyons, 2004). From now on it is not sufficient to look only on positive frequencies but on both the negative and positive frequency axis.

The next step in the DDCv3 when IF $\neq 0$ Hz is the filter step. Using the DDCv3 the signal to be digitised typically is a signal at an intermediate frequency equal to ν_{if}. After the downconversion step half of the signal of interest is around $\nu = 0$ Hz. The second half is at $\nu = -2 \cdot \nu_{\mathrm{if}}$ and any parasitic DC offset of imperfect ADCs is at $\nu = -\nu_{\mathrm{if}}$. As we are interested in the information that is at $\nu = 0$ Hz (after the downconversion) it is necessary to filter out the other frequencies, mainly $\nu = -\nu_{\mathrm{if}}$ and $\nu = -2 \cdot \nu_{\mathrm{if}}$. This is

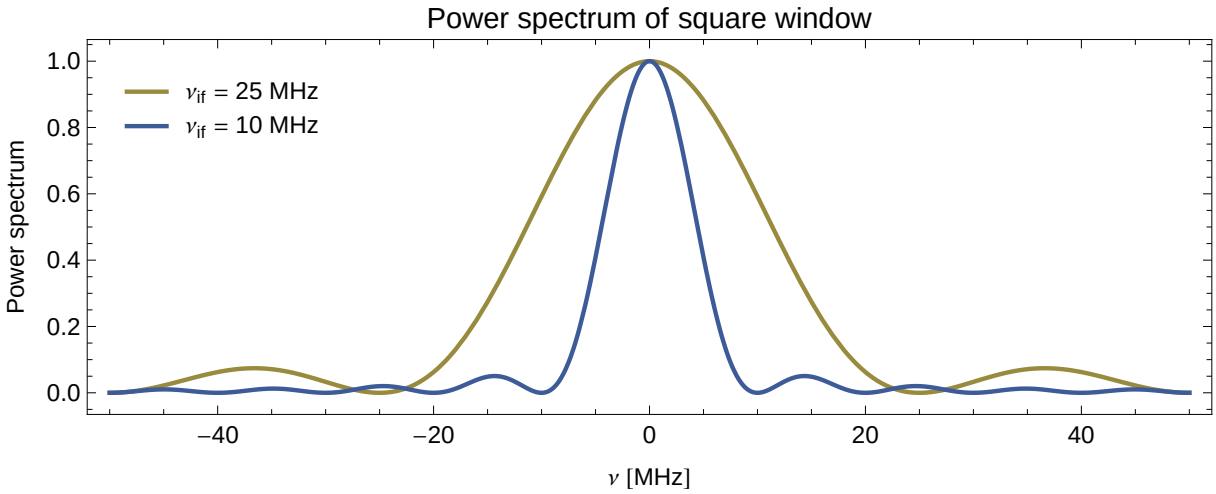


Figure 4.6: Normalised power spectrum of DTFT of square windows used in DDCv3.

done in the DDCv3 by a convolution of the $x_{\mathrm{downc}}(t_n)$ with a square window

$$h_{\mathrm{hom}}(t_n) = \begin{cases} \frac{1}{N}, & \text{for } -(N-1) \leq n \leq 0, \\ 0, & \text{else.} \end{cases}$$

of length $N = {}^{f_s}/_{\nu_{\mathrm{if}}}$ and height ${}^{1}/_{N}$. This digitally homodyned data $x_{\mathrm{hom}}(t_n)$ are the output of the DDCv3:

$$x_{\mathrm{hom}}(t_n) = \frac{1}{N} \cdot \sum_{j=0}^{N-1} x_{\mathrm{downc}}(t_{n-j}).$$

A convolution of two time domain signals (here the signal $x_{\mathrm{downc}}(t_n)$ and the square window $h_{\mathrm{hom}}(t_n)$) is equivalent to a multiplication of their complex Fourier spectra, $X_{\mathrm{downc}}(\nu)$ and $H_{\mathrm{hom}}(\nu)$, in the frequency domain. So the resulting Fourier spectrum is:

$$X_{\mathrm{hom}}(\nu) = X_{\mathrm{downc}}(\nu) \cdot H_{\mathrm{hom}}(\nu).$$

In Figure 4.6 the normalised power spectra

$$\frac{|H_{\mathrm{hom}}(\nu)|^2}{|H_{\mathrm{hom}}(0)|^2} = \left(\frac{1}{N} \cdot \frac{\sin\left(\pi \frac{\nu}{f_s} N\right)}{\sin\left(\pi \frac{\nu}{f_s}\right)} \right)^2$$

of the square windows for two possible IFs are shown. The normalised power spectra are chosen because they show the ratio of the remaining power before and after the convolution. The important zero points at $\nu = -\nu_{\mathrm{if}}$ and $\nu = -2\,\nu_{\mathrm{if}}$ can be seen. Any parasitic DC offset in the signal $x_{\mathrm{dig}}(t_n)$ is filtered out by the first zero point and the second filters out the double frequency term of $x_{\mathrm{downc}}(t_n)$. The area under the power spectra is exactly ν_{if} in the normalisation used. Multiplying this power spectrum with the power

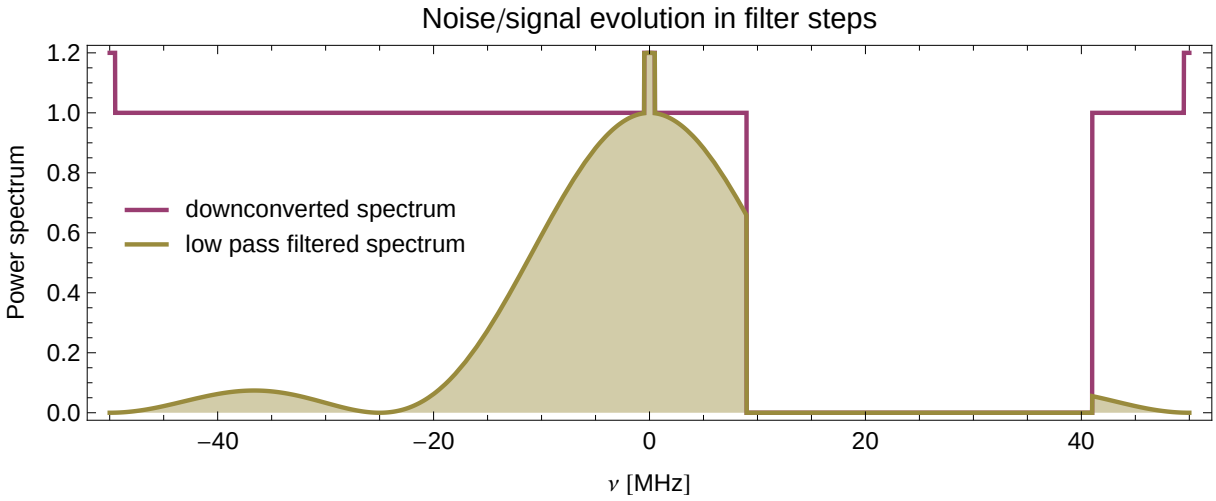


Figure 4.7: Example power spectrum after the whole homodyning process.

spectrum example of Figure 4.5 results in the power spectrum shown in Figure 4.7 for $\nu_{\text{if}} = 25\,\text{MHz}$. The overall remaining power after the homodyning process is shown by the shaded area where the power at $\nu = -\nu_{\text{if}}$ (parasitic DC offset of the ADCs) and $\nu = -2\,\nu_{\text{if}}$ is filtered out completely. After this procedure the data are returned at the output of the DDCv3 as $x_{\text{hom}}(t_n) = I_{\text{hom}}(t_n) + i\,Q_{\text{hom}}(t_n)$. For an experimental observation of the digital downconversion steps (digitising, downconversion, low pass filtering) described above see Section 5.2.

If the tricky downconversion $\text{IF}_{01} = 25\,\text{MHz}$ is selected for the DDCv3 all the downconversion steps are the same as described above. The only difference is that a specific global phase offset $\varphi = 0$ is chosen and the sinusoids are nothing else then $1, 0, -1, 0, \ldots$ with $\nu_{\text{if}} = 25\,\text{MHz}$ and the sampling rate $f_s = 100\,\text{MHz}$. The multiplication by -1 can be performed by just flipping some bits and lasts therefore "no" time. In this method the downconverted data $x_{\text{hom}}(t_n) = I_{\text{hom}}(t_n) + i\,Q_{\text{hom}}(t_n)$ is delivered instantaneously to the output of the DDCv3 whereby the normal downconversion lasts 30 ns which is the time for the arbitrary multiplication.

If $\text{IF}_{10} = 0\,\text{Hz}$ is selected for the DDCv3 the data of ADC1 and ADC2 is just delivered and returned at the output of the DDCv3. The output of the DDCv3 in this case is:

$$x_{\text{hom}}(t_n) = x_{\text{dig,ADC1}}(t_n) + i\,x_{\text{dig,ADC2}}(t_n) = I_{\text{hom}}(t_n) + i\,Q_{\text{hom}}(t_n).$$

Alternatively I_{hom} and Q_{hom} are swapped when bit 2 is set to 1.

4.4.2 Grabber v03

The Grabber v03 (Grabv3) writes the data of the ADCs and the four user pins in the RAM specified by register one. After activating the application the grabbing begins with the start trigger (specified by DDCv3) and ends after 'grab points' are stored in the RAM.

The number of grab points is given as a parameter through bits 0 to 18 of register six. Since the are only 19 bits of addresses in each bank of RAM the maximum time for grabbing data is $t_{\max} = 2^{19} \cdot 10\,\text{ns} = 5.24288\,\text{ms}$. The Grabv3 is started by assigning at least one bank of RAM to application 4 using register one as described in Section 4.3.

As an alternative grabbing source I and Q from the DDCv3 can be used by setting bit 19 of register six to 1. The parameters to setup the DDCv3 correctly are described in Section 4.4.1.

4.4.3 Averager v04

The Averager v04 (AVGv4) performs an ensemble average measurement of J single experiments. Hereby the quadrature signal digitised by the ADCs is averaged as described in this section.

Parameters

The time discrete (time points t_n after the start trigger) quadrature signal to be averaged comes from the DDCv3 which therefore needs to be initialised appropriately, compare Section 4.4.1. The AVGv4 is parametrised by register seven. Bits 12 to 31 (decoded as an unsigned integer value) give the number of shots J to be averaged and bits 0 to 11 give the number of time points N (namely the time $t_N = {}^{N}/_{f_s} = N \cdot 10\,\text{ns}$ is averaged) after the start trigger. More precisely the AVGv4 waits for a positive edge of the start trigger. This positive edge sets the time point t_0 and the shot number $j = 0$.

Concept

When the time point t_0 is set the AVGv4 processes the quadrature signal $x_j(t_n) = I_j(t_n) + i\,Q_j(t_n)$, that leaves the DDCv3 for shot j for all time points $t_0, \ldots, t_{N-1}$. After the time point t_{N-1} the application sets itself into idle waiting for the next positive edge of the start trigger. This resets the time point t_0 and the next shot number $j \leftarrow j + 1$ is processed and so on until shot $j = J - 1$ is completed and the AVGv4 terminates itself. At the end the averaged quadrature signal

$$x_{\text{avg}}(t_n) = \sum_{j=0}^{J-1} x_j(t_n) = \sum_{j=0}^{J-1} I_j(t_n) + i \sum_{j=0}^{J-1} Q_j(t_n) = I_{\text{avg}}(t_n) + i\,Q_{\text{avg}}(t_n),$$

is computed for time points $t_0, t_1, \ldots, t_{N-1}$. The outcomes for $I_{\text{avg}}(t_n)$ and $Q_{\text{avg}}(t_n)$ are written to the external RAMs of the FPGA card using the time point number n as the address number. As the block RAM on the "user FPGA" is limited the maximum number of possible time points is limited to 4 096 in this version. To get the real averaged

quadrature signal

$$\frac{1}{J} \cdot \sum_{j=0}^{J-1} x_j(t_n) = \tfrac{1}{J}\, I_{\mathrm{avg}}(t_n) + i \cdot \tfrac{1}{J}\, Q_{\mathrm{avg}}(t_n)$$

the outcomes of the AVGv4 $I_{\mathrm{avg}}(t_n)$ and $Q_{\mathrm{avg}}(t_n)$ need to be divided by the number of shots J.

Start-up

The AVGv4 consists of two applications, application 6 computing $I_{\mathrm{avg}}(t_n)$ and application 7 (compare Figure 4.4) computing $Q_{\mathrm{avg}}(t_n)$. To start the AVGv4 both banks of RAM are assigned to application 6 and 7 respectively by setting up register one appropriately as described in Section 4.3 and visualised in the block diagram of Figure 4.4. If only one quadrature, $I_{\mathrm{avg}}(t_n)$ or $Q_{\mathrm{avg}}(t_n)$, is of interest it is sufficient to assign only one bank of RAM to application 6 or 7 respectively.

4.4.4 Single Shot Simple v03 and Single Shot Arbitrary v04

The Single Shot Simple v03 (SSSv3) and Single Shot Arbitrary v04 (SSAv4) applications calculate a score for every single shot measurement. The single shot measurements are implemented as proposed by Gambetta et al. (2007) to read-out the qubit state in circuit QED. Here SSSv3 performs the box car linear filter and SSAv4 can be set up to perform the exponential decaying linear filter or the optimal linear filter, as they were stated in Gambetta et al. (2007).

Parameters

The two applications are parametrised over register five and register three respectively. Bits 0 to 12 indicate the number of integration points N and bits 13 to 31 specify the number of shots J to be processed. Bits 0 to 28 of register four signalise both applications the starting point of the integration. More precisely the raising edge sets the current time back to t_{-K}. Then the integration starts at time t_0 and goes until t_{N-1}. Further the DDCv3 needs to be initialised appropriately (see Section 4.4.1) as the quadrature signal $x_j(t_n) = I_j(t_n) + i\, Q_j(t_n)$ leaving the DDCv3 is analysed by the SSSv3 and the SSAv4. After activating, the applications wait for the raising edge of the start trigger while the shot trigger sets t_{-K}.

Concept

In the case of the SSSv3 the data of each shot is summed up from t_0 to t_{N-1}, where the number of integration points is reached, to calculate the box car integrated single shot

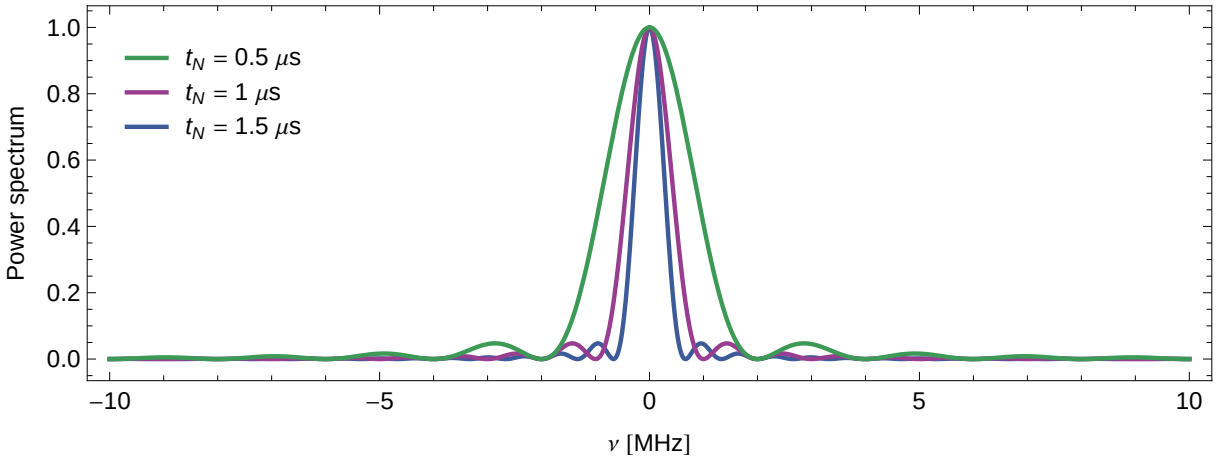


Figure 4.8: Normalised power spectra of the DTFT of square windows used in the SSSv3.

score

$$s_{j,\mathrm{SSSv3}} = \sum_{n=0}^{N-1} x_j(t_n) = \sum_{n=0}^{N-1} I_j(t_n) + i \sum_{n=0}^{N-1} Q_j(t_n) = s_{j,I} + i\, s_{j,Q}.$$

Every raising edge of the shot trigger resets t_{-K} and starts a new score calculation for $j \leftarrow j+1$. When the integration for score s_{J-1} is completed SSSv3 terminates. All the scores $s_{j,\mathrm{SSSv3}}$ are stored in the external RAM of the FPGA card using the shot number $j = 0, \ldots, J-1$ as address. The scores $s_{j,I}$ and $s_{j,Q}$ are rounded to a 16 bit signed 2's complement fixed point number with the binary point at bit 11 before $s_{j,I}$ is stored in the first 16 bits of address j and $s_{j,Q}$ in the last 16 bits (one half of the width of each memory address).

The difference of the SSAv4 to the SSSv3 is that the SSAv4 application performs a multiplication with $k(t_n)$, called kernel, before the numerical integration:

$$s_{j,\mathrm{SSAv4}} = \sum_{n=0}^{N-1} k(t_n) \cdot x_j(t_n) = \sum_{n=0}^{N-1} k(t_n) \cdot I_j(t_n) + i \sum_{n=0}^{N-1} k(t_n) \cdot Q_j(t_n) = s_{j,I} + i\, s_{j,Q}.$$

Here the data stored at the end of the RAM is used as kernel $k(t_n)$. The first factor $k(t_0)$ must be stored by the user as a 32 bit 2's complement fixed point number with a fraction length of 13 bits at address $2^{19}-1$, the second factor $k(t_1)$ at address $2^{19}-2$, etc. This process is called an arbitrary linear filter as every possible linear filter function could be implemented by just designing the correct kernel and writing it into the RAM.

Equally as the DDCv3 (see Section 4.4.1) the SSSv3 and SSAv4 can be considered as a digital filter. In the case of the SSSv3 the digital filter is a square window filter of length $t_N = {}^{N}/_{f_s} = N \cdot 10\,\mathrm{ns}$. Figure 4.8 shows the power spectra of such square windows with different box car integration times t_N. As can be easily seen the SSSv3 filters out the zero frequency component of the measurement signal. The pass band becomes narrower the longer the integration time t_N is. In the case of the SSAv4 the power spectrum is

$|K(\nu)|^2$ where $K(\nu)$ is the DTFT of the kernel $k(t)$. The product of $|K(\nu)|^2$ and the power spectrum of the data that leave the DDCv3 is the power spectrum remaining after the SSSv3 or the SSAv4.

Start-up

The SSSv3 or the SSAv4 are started by assigning a bank of RAM to application 2 or application 4 respectively using register one as described in Section 4.3. As both applications only need one bank of memory they can be started simultaneously. In the case of starting the SSAv4 it is important to ensure that the correct kernel is written to the RAM the SSAv4 is assigned to.

4.4.5 Write Memory v01

The program Write Memory v01 is a very small program. All the RAM banks assigned to the program are deleted at the system clock rate of 100 MHz and the value zero is written to all addresses. The deleting process only lasts $t = 2^{19} \cdot 10\,\text{ns} = 5.24288\,\text{ms}$ in total. To start the memory clearing process the banks of RAM, that should be deleted, are assigned to the Write Memory v01 application 3 via register one (see Section 4.3). When the memory is cleared the application stops and the status changes from running to finished indicated by register eleven (see Section 4.3).

4.5 Library

For being able to control the FPGA card out of the program LabVIEW (or even other programs able to call library functions, such as Matlab) a C-library was implemented making use of the FUSE development API for C/C++ (Nallatech, 2006b). Before being able to take control over the FPGA card a connection must be established to the FPGA. This is done by the function:

`int opencard (`*LOCATE_HANDLE* `*hLocate,` *DIME_HANDLE* `*hCard,`
int `verbose)`
This function establishes a connection to the FPGA card.

- `*hLocate` is an empty handle of type *LOCATE_HANDLE* where the connection parameters are stored.
- `*hCard` is an empty handle of type *DIME_HANDLE* where the connection parameters to the "BenADDA" board are stored.
- `verbose` boolean (0/1) to indicate whether information should be printed.

The function `opencard` ensures that no other programs are able to connect themselves to the same FPGA card. The handles `*hLocate` and `*hCard` need to be saved as they are necessary to close the connection. The `*hCard` is important for every function to be

evaluated in the following because it holds the connection information in which DIME slot the "BenADDA" is located. A second function `opencardRemote` establishes a remote "PCI" connection to the FPGA over the LAN. However, this process gets slow when transferring data from or to the FPGA card. When the control is no longer needed the connection should be closed to make it accessible for other programs. If the connection is not closed appropriately the FPGA card is blocked until the library is unloaded from the PC memory. The connection is closed by the function:

`int closecard (`*LOCATE_HANDLE* `*hLocate,` *DIME_HANDLE* `*hCard,` *int* `verbose`)
This function closes the connection to the FPGA card.

`*hLocate` is the connection handle to the FPGA card that should be closed.

`*hCard` is the handle to the "BenADDA" board that should be closed.

`verbose` boolean (0/1) to indicate whether information should be printed.

The FPGA connection is hereby made accessible for new programs. To program the "clock FPGA" and "user FPGA" on the FPGA card the function

`int programcard (`*DIME_HANDLE* `*hCard,` *char* `*clockfile,` *char* `*programfile,` *double* `*clockFreq,` *int* `verbose`)
This function programs the FPGAs on the FPGA card and sets some software programmable clocks.

`*hCard` is the handle to the "BenADDA" board that should be programmed.

`*clockfile` gives the path including the ".bit" file that should be programmed on the "clock FPGA".

`*programfile` gives the path including the ".bit" file that should be programmed on the "user FPGA".

`*clockFreq` sets three software programmable clocks amongst others the clock for the "PCI FPGA". The other clocks are not used in the case the "clock FPGA" is programmed with the program described in Section 4.3.

`verbose` boolean (0/1) to indicate whether information should be printed.

is used.

In the case in which the "user FPGA" is programmed with the "wrapper" described in Section 4.3 the library provides further basic functions to communicate with the "wrapper" that is part of the "user FPGA":

`int writeMemoryDIME (...)`: This function writes static data into the specified addresses of the specified RAM.

`int writeMemoryArrayDIME (...)`: This function writes a given array interpreted as unsigned 32 bit integers into the specified addresses of the specified RAM.

`int readMemoryDIME (...)`: This function reads out the RAM at given addresses and saves the data as unsigned 32 bit integers into a specified file.

`int writeUserRegister (...)`: This function writes a given unsigned 32 bit integer into the specified register one to eleven.

`int readUserRegister (...)`: This function reads the data of the specified register one to eleven into a given pointer address with width 32 bit.

In the case in which the "user app component" is included in the "wrapper" with the applications described in Section 4.4 running, there are amongst others the following top level functions available in the library to initialise the applications appropriately, to request their status and to start and stop them with the correct RAM bank assignment:

`int setupDownconversion_03 (...)`: This function setups the DDCv3 writing the parameters into the correct bits of the correct registers as described in Section 4.4.1.

`int setupGrabber_03 (...)`: This function setups the Grabv3 writing the parameters into the correct bits of the correct registers as described in Section 4.4.2.

`int setupAverager_04 (...)`: This function setups the AVGv4 writing the parameters into the correct bits of the correct registers as described in Section 4.4.3.

`int setupSingleShotSimple_03 (...)`: This function setups the SSSv3 writing the parameters into the correct bits of the correct registers as described in Section 4.4.4.

`int setupSingleShot_04 (...)`: This function setups the SSAv4 writing the parameters into the correct bits of the correct registers as described in Section 4.4.4.

`int giveStatusForApps (...)`: This function returns the running status for two requested application numbers. A return value of zero specifies that both applications have finished, one represents that the first application is still running, two that the second is still running and three that both are still running. Values greater than three indicate an error while reading the register.

`int startApps (`*DIME_HANDLE* `*hCard,` *int* `zbt1appNum,` *int* `zbt2appNum`): This function starts application *`zbt1appNum`* assigning access to RAM bank one and application *`zbt2appNum`* assigning access to RAM bank two. In the case in which application zero is specified no application is started. In addition to starting the applications, access for the requested banks of RAM is switched from the PC to the FPGA. The PC is then no longer able to read or write these banks of RAM until the function `stopApps` is called.

`int stopApps (...)`: This function stops all applications running in the "user app component" and switches the access to all banks of RAM back to the PC.

Using the top level functions, described above, a LabVIEW program is implemented which runs on the PC the FPGA is installed in. This program is able to perform FPGA measurements and to save the measurement data on this PC, compare Figure 4.9. By the Cleansweep program, which controls the measurement apparatus including the long established Acqiris data acquisition card, this LabVIEW program can be called remotely (making use of the "LabVIEW VI Server"). Called by the Cleansweep program the FPGA card measurement runs in parallel to the Acqiris card measurement.

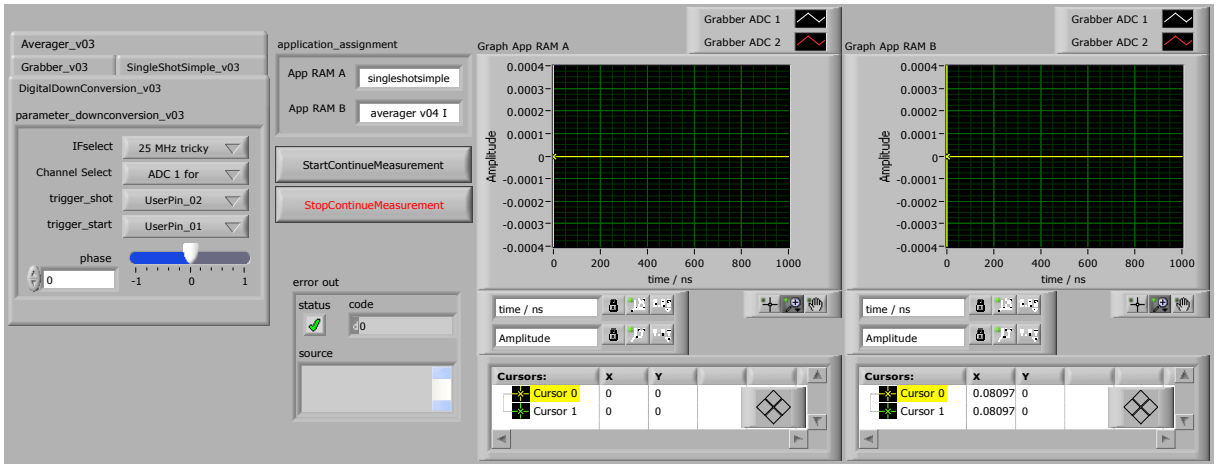


Figure 4.9: LabVIEW program controlling the applications running in the "user app component". When the program is started a connection to the FPGA is established. Before a measurement is started the applications are initialised with the specified parameters. Then the measurement is started by assigning the defined bank of RAM to the specified applications. When the measurement is completed the applications are stopped, the RAM is assigned back to the PC, the measurement data is read out of the RAMs and stored on the disk. At the end the data is read, interpreted and displayed appropriately in the graphs. When the program is closed the connection to the FPGA is freed.

Chapter 5

FPGA verification

The last chapter introduced the FPGA card, its hardware and the programmed digital signal processing and analysis applications. In this chapter I will experimentally characterise the relevant hardware and verify the applications running on the FPGA. For setting up a reliable system it is important to check the correct functionality. In the first section the anti-aliasing filter which is in front of the ADCs is characterised. It turns out that this built-in filter is not sufficient to prevent aliasing in our system. However, this can easily be solved. Section 5.2 analyses theoretically the evolution of noise in the DDCv3 (compare Section 4.4.1) on the basis of real data recorded by a spectrum analyser. The result is compared to experimental data that passed through the ADC and the DDCv3 on the FPGA card resulting in very good agreement. Finally in Section 5.3 measurements are performed simultaneously with a long established data acquisition board and the new FPGA card to verify the consistency with existing measurement routines.

5.1 ADC input filter

The inputs of the FPGA to the ADCs provide a single ended to differential conversion. In the same circuit a 3rd-order passive anti-aliasing filter with -3 dB point at 58 MHz is implemented, see Nallatech (2006a). The input filter characteristic can be resolved by generating sine waves at different frequencies (frequency step size $\approx$ 1.5 MHz) and measuring the attenuation of their amplitudes by fitting a sine of the corresponding frequency to the digitised data. See Figure 5.1 for a sketch of the experimental setup. The analysis of the fitted data results in the filter characteristic shown in Figure 5.2. A slight amplifi-

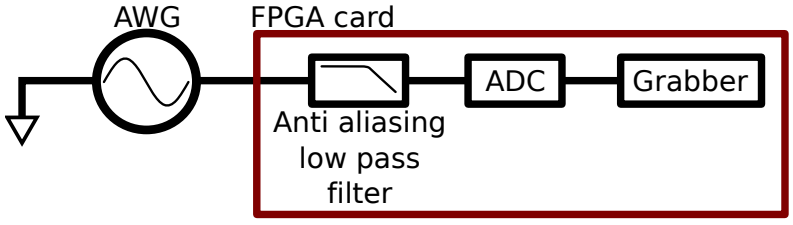


Figure 5.1: Sketch of the experimental setup to characterise the permanent mounted ADC input filter on the FPGA card.

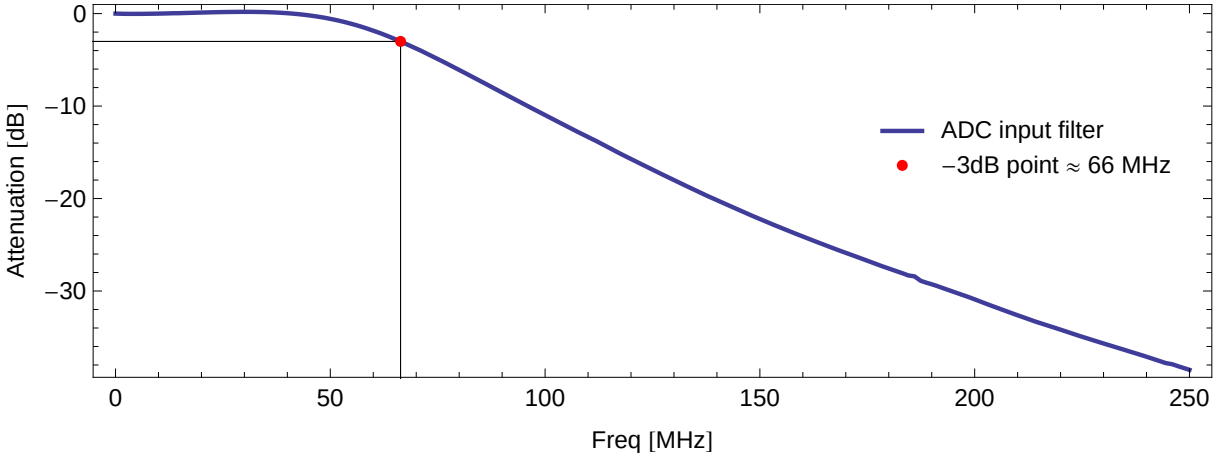


Figure 5.2: Anti-aliasing filter characteristic of the input to the ADCs in the FPGA card. The attenuation is given in power, whereby the data is obtained with a frequency resolution of $\approx 1.5\,\mathrm{MHz}$.

cation around 30 MHz indicates that there are not only passive components in the input filter as in the datasheet (Nallatech, 2006a) mentioned. Additionally the -3 dB point is observed around 66 MHz instead of the denoted 58 MHz (Nallatech, 2006a).

5.2 Noise evolution in the digital downconversion

Noise is produced by means of an AWG by generating Gaussian distributed random values at a sample rate $f_{s,\mathrm{AWG}} = 1.25\,\mathrm{GHz}$. Due to the Nyquist theorem the highest frequency component of this noise reaches up to $f_{s,\mathrm{AWG}}/2$. To get a well defined noise spectrum it is filtered first with a passive 105 MHz and then with a passive 30 MHz filter. These two noise spectra are analysed by a spectrum analyser and digitised by the FPGA card at a sampling rate of $f_s = 100\,\mathrm{MHz}$. Figure 5.3 shows the experimental setup. In Figure 5.4 the spectrum analyser data is shown for the two different low pass filter. The spectrum analyser data is multiplied with the ADC input filter coefficients because this is the spectrum the ADC in the FPGA card receives as a time domain signal (compare Figure 5.3). Additionally the spectra are divided by two and mirrored to get power bins on the negative and positive frequency axis so that they can be compared later with complex Fourier spectra. Figure 5.4 shows the resulting spectra in blue and ochre. Since the Gaussian distributed points are repeated all the time by the AWG there is quasi-noise generated. This explains the noisy aspect of the power spectrum generated by the spectrum analyser, although it was averaged 100 times. When plotting the spectra on a linear scale this effect seems to be even emphasised. This phenomenon is also visible in Figure 5.5 and 5.6. DC offsets either from the AWG or the spectrum analyser cause a large power bin at DC, clearly visible in Figure 5.4 and also in Figure 5.5 and 5.6. As the ADC samples its input at $f_s = 100\,\mathrm{MHz}$, power in frequency bins higher than the Nyquist frequency $f_s/2$ is folded back into the lower frequency band $-f_s/2$ to $f_s/2$ (Lyons,

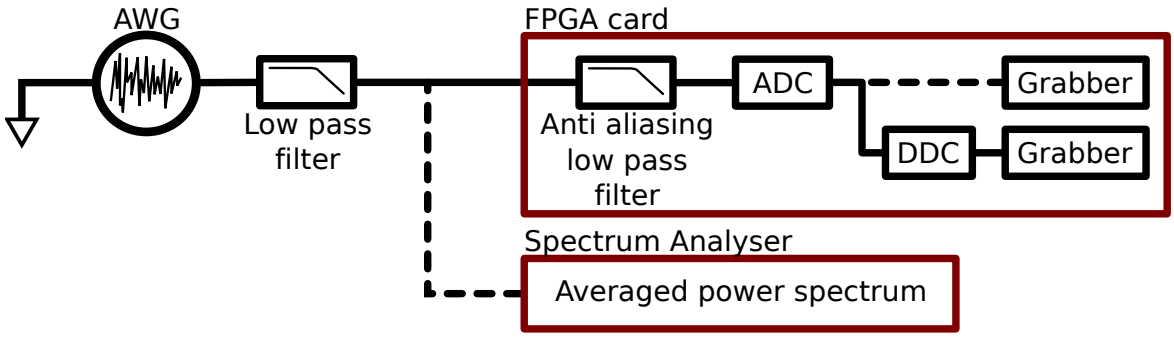
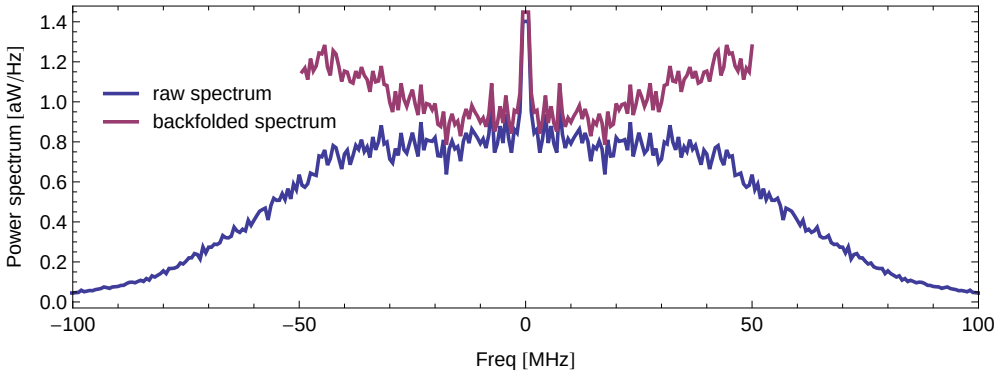


Figure 5.3: Sketch of the experimental setup used in this chapter to study noise. The AWG is set up to generate white noise which is filtered by two different passive low pass filter. The resulting signal is analysed once with a spectrum analyser and once it is digitised by the ADC on the FPGA card. Hereby, once the raw digitised signal is recorded by the Grabber (Grabv3, Section 4.4.2) and once the digitised signal passes the digital downconverter (DDCv3, Section 4.4.1) before it is recorded by the Grabv3.

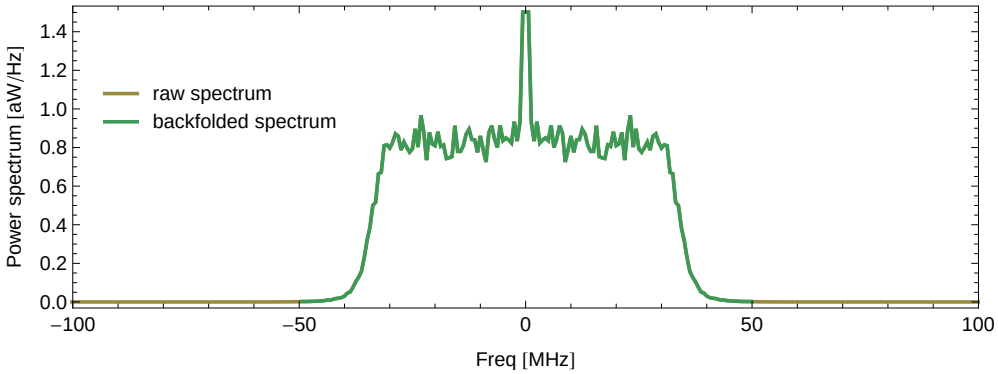
2004). Hereby the power in bin 51 MHz is added to the power in bin 49 MHz, 52 MHz to 48 MHz, etc. An intuitive explanation is that to the time discrete values of a sine wave with frequency 60 MHz sampled at 100 MHz a sine wave of 40 MHz can be perfectly fit. This effect can be also seen at very fast rotating car wheels. They seem to rotate backwards. However, this is a visual illusion, because pictures are delivered at a too low rate to the brain. Due to aliasing, power in frequency bins higher than the Nyquist frequency of $f_s/2$ is backfolded into lower frequency bins which is clearly visible in the noise spectrum filtered with the 105 MHz low pass filter (purple in Figure 5.4(a) and 5.4(c)). This effect is almost not visible in the 30 MHz filtered data (ochre in Figure 5.4(b) and 5.4(c)) as there is nearly no power in higher frequency bins than the Nyquist frequency. Very small backfolding effects can be seen in the logarithmic scale picture (bottom graph of Figure 5.4(c)). It is obvious that the additional anti-aliasing filter of 30 MHz (in this example) is needed to avoid mixing of various frequency components. This backfolded power spectrum is the spectrum we expect to enter the FPGA in form of digital values.

The spectrum of the white noise filtered with the 105 MHz filter is shown on a linear scale in Figure 5.5 as the "raw spectrum" we expect to enter the FPGA. By means of this figure all steps of the digital downconversion will be explained.

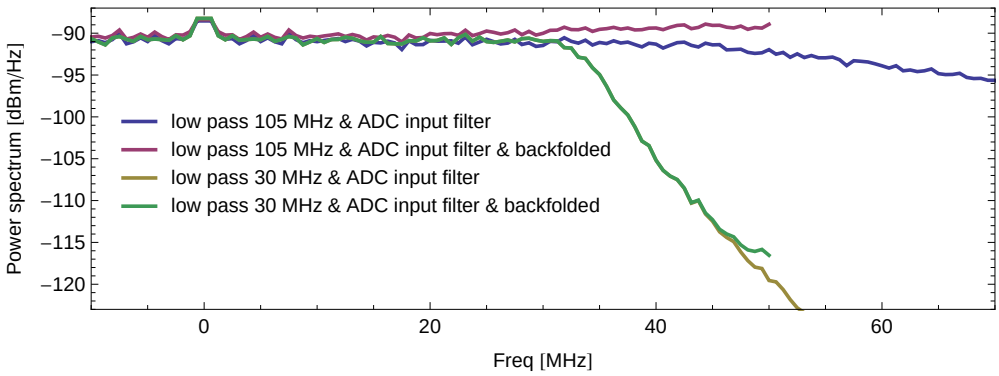
In the first step of the DDDv3 4.4.1 the data (we expect with the "raw spectrum" (blue) in Figure 5.5) is multiplied with a cosine wave and a negative sine wave with fixed phase offset and the specified frequency $\nu_{\text{if}} = 25\,\text{MHz}$ in this case. The data results to be the I and Q quadratures of the signal. A Fourier transform of $I+iQ$ leads to the downconverted spectrum (purple spectrum in Figure 5.5). Here all frequency components are shifted to the left by ν_{if} and showing up on the positive frequency axis because the spectrum of finite discrete time Fourier transform (DTFT) is periodic or circular with period or length of the sample rate f_s (Lyons, 2004). Since this is no real input for the Fourier transform the spectrum is not symmetric around the zero frequency any more and it is necessary to take into account from now on all the frequencies including the negative ones. So the



(a) White Gaussian noise filtered with a 105 MHz low pass filter



(b) White Gaussian noise filtered with a 30 MHz low pass filter



(c) Figure 5.4(a) and 5.4(b) joined on a logarithmic scale

Figure 5.4: Power spectra of filtered white Gaussian noise. As we are interested in the power spectrum that is digitised by the ADC on the FPGA card, the spectra analysed by the spectrum analyser are multiplied with the ADC input filter coefficients (Figure 5.2). Further the resulting spectra are multiplied with $1/2$ and mirrored onto the negative frequency axis, resulting in the "raw spectrum", for illustration purposes as we want to compare them with complex power spectra. Aliasing at ± 50 MHz results in the "backfolded spectrum". Plots (a) and (b) show the complex power spectra for a 105 MHz and a 30 MHz low pass filter behind the white Gaussian noise source (AWG). The curves are joined on a logarithmic scale in plot (c) using the same colours.

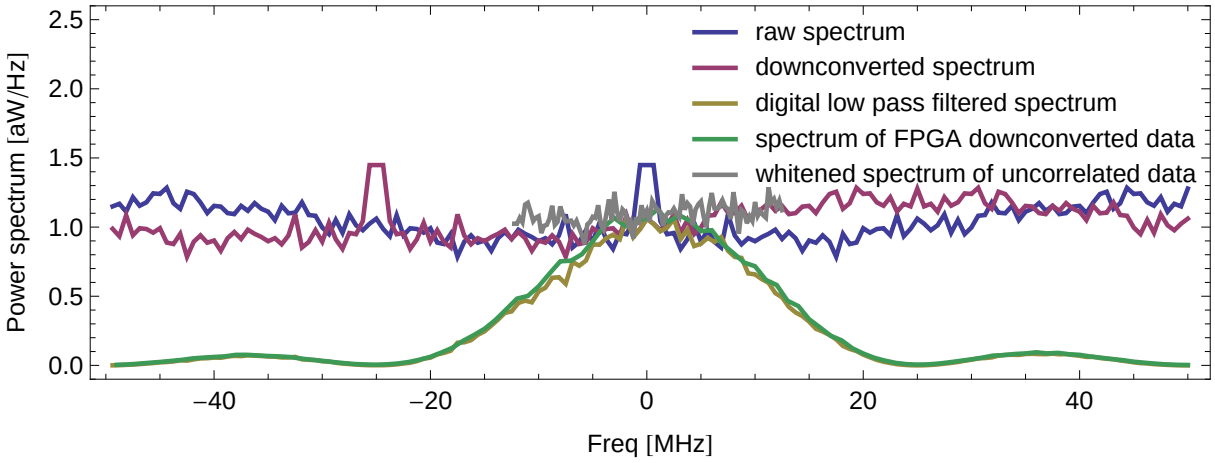


Figure 5.5: Frequency domain evolution ("raw", "downconverted" and "digital low pass filtered" spectrum) of noise in digital downconversion and comparison to the "digitally downconverted" (by the DDCv3) data experimentally observed with the FPGA (spectrum of FPGA). "Whitened spectrum" of uncorrelated data is the spectrum obtained using only every f_s/ν_{if} time point (often applied to reduce data). Here white noise of bandwidth 105 MHz filtered by the ADC input filter at the FPGA card and digital downconverted from $\nu_{\text{if}} = 25\,\text{MHz}$ by the DDCv3 is investigated.

spectrum we expect after this first step in the DDCv3 is the "downconverted spectrum" (purple) in Figure 5.5.

The next step is the low pass step where the data is averaged by a sum over the last f_s/ν_{if} samples. This can be interpreted also as a convolution of the data with a square window of length f_s/ν_{if}. A convolution is the multiplication of the two Fourier transforms of the two convoluted data sets in the frequency domain. The Fourier transform of the square window corresponding to our sampling rate f_s and intermediate frequencies $\nu_{\text{if}} = 25\,\text{MHz}$ and $\nu_{\text{if}} = 10\,\text{MHz}$ is shown in Figure 4.6 of Section 4.4.1, where the theoretical operation mode of the digital downconverter is explained. The "downconverted spectrum" is multiplied by this square window spectrum resulting in the "digital low pass filtered spectrum" (ochre) shown in Figure 5.5. This is the spectrum we expect to leave the DDCv3. The DC components that entered the FPGA originally are filtered out completely. Equally half of the original ν_{if} component located at $-\nu_{\text{if}}$ and then downconverted to $-2\,\nu_{\text{if}}$ is filtered out.

To compare the spectrum obtained in the last paragraph (ochre in Figure 5.5) to the data that is digitised with the ADCs of the FPGA card, the downconverted data (performed by the FPGA with the DDCv3) is used and a Fourier transform is performed. Since a single Fourier transform on the whole data set would result in a single high resolution spectrum, the time discrete data was divided into several smaller windows to perform a noiseless averaged Fourier transform. On each window consisting of 100 points a DTFT is performed and the resulting power spectra are averaged. As expected, the resulting power "spectrum of the FPGA downconverted data" (green spectrum in Figure 5.5) is

very similar to the "digital low pass filtered spectrum" (compare green and ochre curves in Figures 5.5, 5.6(a), 5.6(b) and 5.6(c)).

The last spectrum (gray, "whitened") in Figure 5.5 is the spectrum obtained from the DTFT by only taking every f_s/ν_{if}-th data point, here every fourth data point, into account. Neighbouring data points that have processed the digital downconversion have $f_s/\nu_{\text{if}} - 1$ summands in common. Therefore they are strongly correlated. The next but one neighbouring data points have $f_s/\nu_{\text{if}} - 2$ summands in common and so on until the next but f_s/ν_{if} have no summands in common anymore. The total power (integral over all frequencies) remains equal for the "whitened" (gray) and the normal DTFT power spectrum (green) but most of the correlation gets lost. As long as these correlations are not of interest often there is saved only every f_s/ν_{if}-th data point for storage reasons.

The same analysis as performed for Figure 5.5 are done for the three remaining data sets. Figure 5.6(a) shows the analysis of 30 MHz low pass filtered noise and $\nu_{\text{if}} = 25\,\text{MHz}$. For this set of parameters, that are mainly used in the experiments presented in this thesis, the asymmetry of the noise power around DC is clearly visible confirming that the quadrature signal is analysed properly.

The same procedure is performed using $\nu_{\text{if}} = 10\,\text{MHz}$ resulting in similar plots (Figure 5.6(b) for 105 MHz low pass filtered noise and 5.6(c) for 30 MHz low pass filtered noise) with narrower downconversion filter bandwidth leading to smaller noise power in the downconverted signal.

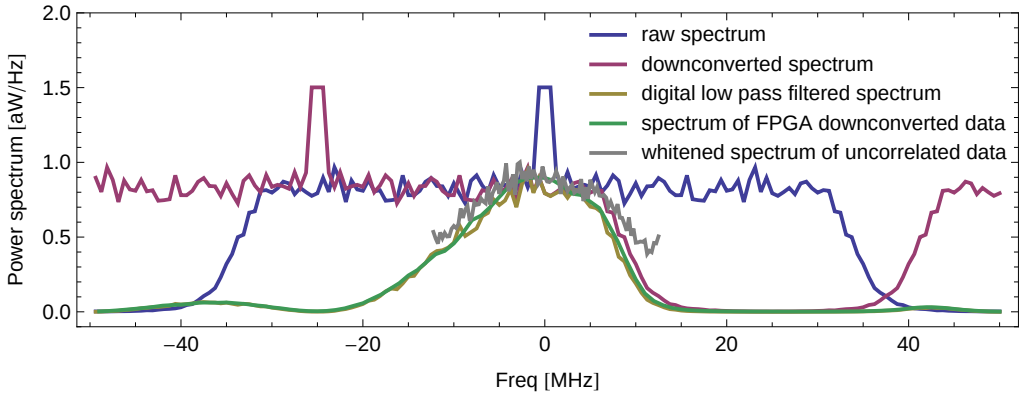
5.3 Comparison of long established AQC and new FPGA data acquisition

In this section the measurements with the FPGA card are compared to measurements with the long established professional Acqiris card (AQC) that has been integrated in the measurement setup up to now. First the internally generated noise of the two cards is investigated. In the consecutive section time resolved measurement routines are compared.

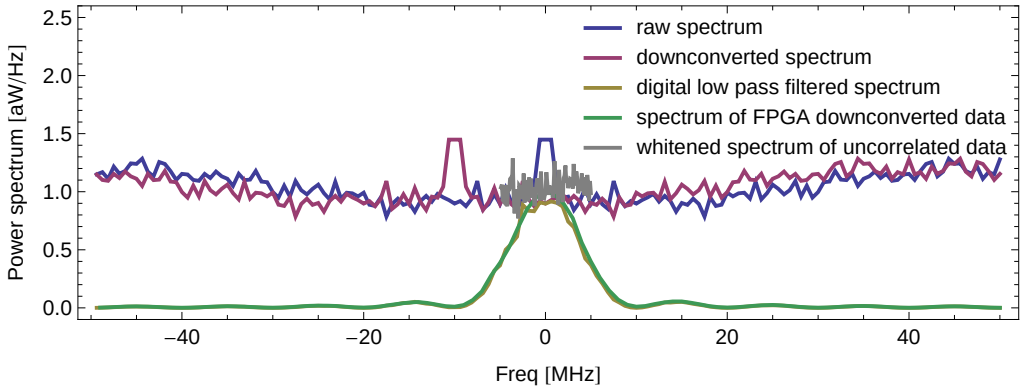
5.3.1 Correlated noise

The correlated noise, that cannot be averaged out, is investigated on both data acquisition boards, the long established AQC and the FPGA card. For the FPGA card we expect the effective number of bits (ENOB) to be at best 11 (Nallatech, 2006a). The main reason for this worse performance (in comparison to the 14 bit resolution of the ADC and a ENOB of ≈ 13 when clocked by the 105 MHz on-board oscillator (Nallatech, 2006a)) is the external clocking of the ADCs with $f_s = 100\,\text{MHz}$ whereby the reference clock of 10 MHz is divided by ten on the FPGA card.

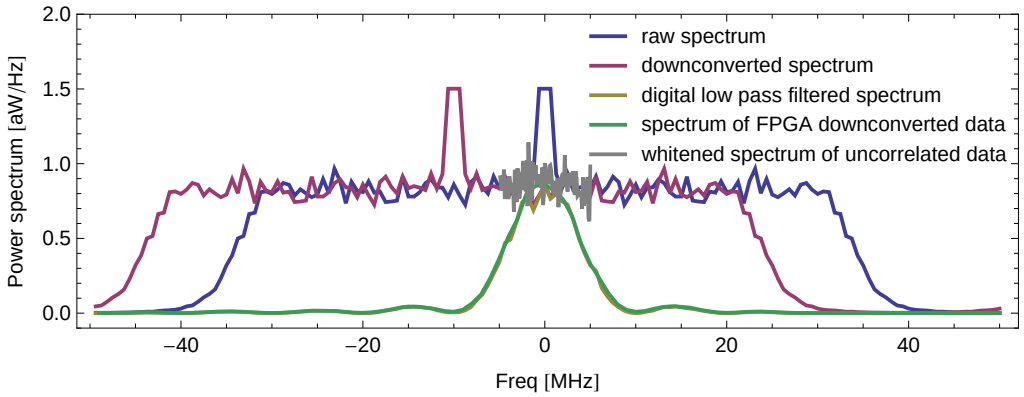
A continuous measurement tone with $\nu_{\text{meas}} = \nu_{\text{res}}$ is sent to the resonator (see Figure 3.3) and the measurement signal $x_j(t_n)$, $t_n = t_0, \ldots, t_N$ ($t_N = 10\,\mu\text{s}$) with $j = 1, \ldots, J$ specify-



(a) White noise 30 MHz low pass filtered and digital downconverted from $\nu_{\text{if}} = 25\,\text{MHz}$.



(b) White noise 105 MHz low pass filtered and digital downconverted from $\nu_{\text{if}} = 10\,\text{MHz}$.



(c) White noise 30 MHz low pass filtered and digital downconverted from $\nu_{\text{if}} = 10\,\text{MHz}$.

Figure 5.6: Frequency domain evolution ("raw", "downconverted" and "digital low pass filtered" spectrum) of noise in digital downconversion and comparison to the "digitally downconverted" (by the DDCv3) data experimentally observed with the FPGA (spectrum of FPGA). "Whitened spectrum" of uncorrelated data is the spectrum obtained using only every f_s/ν_{if} time point (often applied to reduce data). The evolution is illustrated on measured low pass filtered white noise (for different cut-off frequencies) by the spectrum analyser adapted to the expected spectrum entering the FPGA. This can be compared to the FPGA measurement which passed the DDCv3 with the parameter ν_{if}.

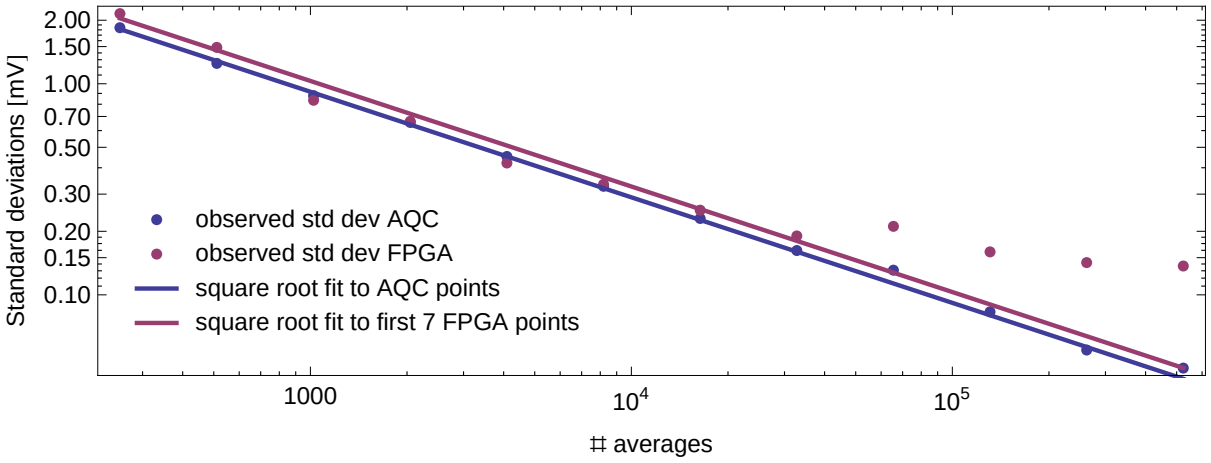


Figure 5.7: Comparison of noise amplitude (standard deviation σ_n) in the Acqiris card (AQC) and the FPGA card. Correlated noise gets visible in the FPGA card around 2^{16} averages.

ing the index for the different shots to be averaged (see Section 4.4.3) for different numbers J of shots. This signal is sent at an intermediate frequency (IF) $\nu_{\text{if}} = 25\,\text{MHz}$. The AQC averages the IF signal which is then downconverted by the Cleansweep program to get the averaged measurement response $a_{\text{AQC}}(t_n)$. In contrast, the FPGA card first downconverts the IF signal with the DDCv3 and then performs the averaging process with the AVGv4 resulting in $a_{\text{FPGA}}(t_n)$. The order of averaging and digital downconversion (DDC) is here not relevant:

$$\begin{aligned} a_{\text{AQC}}(t_n) &= \text{DDC}\left(\frac{1}{J}\sum_{j=0}^{J-1} x_j(t_n)\right) = \frac{1}{n_{\text{if}}} \sum_{n'=n-n_{\text{if}}-1}^{n} \left(\frac{1}{J}\sum_{j=0}^{J-1} x_j(t_{n'})\right) e^{-i\cdot 2\pi\nu_{\text{if}}\cdot t_{n'}} \\ &= \tfrac{1}{J\cdot n_{\text{if}}} \sum_{n'=n-n_{\text{if}}-1}^{n} \sum_{j=0}^{J-1} x_j(t_{n'})\, e^{-i\cdot 2\pi\nu_{\text{if}}\cdot t_{n'}} = \tfrac{1}{J}\sum_{j=0}^{J-1} \left(\tfrac{1}{n_{\text{if}}} \sum_{n'=n-n_{\text{if}}-1}^{n} x_j(t_{n'})\, e^{-i\cdot 2\pi\nu_{\text{if}}\cdot t_{n'}}\right) \\ &= a_{\text{FPGA}}(t_n) \end{aligned} \tag{5.1}$$

where $n_{\text{if}} = {}^{f_s}/_{\nu_{\text{if}}}$. For the two averaged signals, $a_{\text{AQC}}(t_n)$ and $a_{\text{FPGA}}(t_n)$, the standard deviation σ_a in t is calculated. Figure 5.7 shows the comparison of the standard deviations for the AQC and FPGA card measurement. As expected the noise amplitude σ_a averages out with $\sqrt{1/J}$ for low J, compare line fits in Figure 5.7. As illustrated in Figure 5.7 the noise amplitude for the FPGA card starts to saturate at numbers of averages higher than 2^{16} indicating a correlated noise source. The value of $\sigma_a \approx 1.5\,\text{mV}$ seems to be reasonable as it is about one tenth lower than the corresponding voltage error of the ENOB. The AQC shows better performance (at least up to 2^{19}) as it has higher quality ADCs than the FPGA card. When the signal power gets too low, then much more than 2^{16} averages are necessary to examine the measurement signal. The measurement signal becomes superimposed with correlated noise until no measurement signal is observable. The AQC can hereby average more often in order to resolve smaller signal powers. An increased amplification of the measurement signal could increase the possible number of

averages in the FPGA card. In contrast to the averaged measurement the integration of the measurement signal performed by the SSSv3 filters out even the correlated noise as it act as a digital filter, compare Section 4.4.4.

5.3.2 Measurement response

Until now the qubits in the system have been read out via an ensemble average transmission measurement in which the measurement signal was averaged by the AQC over many single experiments. The average capabilities of the FPGA card (AVGv4, Section 4.4.3) and the AQC (similar application as the AVGv4) are compared using the measurement responses obtained first with the qubit in the ground state $|g\rangle$ and then with the qubit in the excited state $|e\rangle$. The shot trigger (compare Section 4.4.1) with a period of $20\,\mu$s triggers the different scenarios. With its raising edge $t_0 = 0\,\mu$s the measurement signal ν_{meas} (see Figure 3.3) is turned off to give the qubit the possibility to relax into its ground state. Shortly before $t = 5\,\mu$s a 13 ns π-pulse is applied through the resonator line to excite the qubit to state $|e\rangle$ if requested. At $t = 5\,\mu$s the measurement signal ν_{meas} is switched on. In the same manner as the measurement and π-pulse are controlled, triggers are distributed to the AQC and the FPGA card. As the FPGA card has a $1/f_s = 10$ ns slot before a raising edge can be detected and the AQC in normal mode a slot of 1 ns, it is crucial not to reset the shot trigger so that the phase relation between the AQC and the FPGA card is fixed. Otherwise the phase relation jumps to a random point in the 10 ns slot.

Figure 5.8 shows a comparison of the averaged measurement response in the AQC and the AVGv4 of the FPGA card. Both measurements were averaged $J = 2^{16} - 1 = 65\,535$ times. As the AQC and the FPGA card get the data from the two different arms of the analog mixer (see Figure 3.3) it is expected that the two data sets have a phase difference of $\approx 90\,^\circ$. In addition, there is a constant phase shift due to a different cable length of the signal after the mixer and the cable length for the triggers. A random phase shift is additionally caused by the different time slots for catching the trigger. For this special measurement a phase difference of $90\,^\circ + 9.5\,^\circ$ is observed. The data is corrected with a constant factor for each card. The correction factor for the FPGA card was found to be $(1.1 \cdot 1.106)$ V in a similar experiment as described in Section 5.1. The full range of the ADCs in the FPGA card is ± 1.1 V with an allowed "gain error" of 10.6 %. The 14 bits encode this full range of the ADCs. The data of the AQC is corrected by $1/2\,1.04$ V as the Cleansweep program multiplies the data by 2 in the downconversion. The correction of 4 % needs not to be a "gain error" but just indicates a correction between the cards or some artefact in the measurement of the FPGA "gain error". As shown in Figure 5.8 the data matches very good with a little more noise in the FPGA data as expected in the previous Section 5.3.1.

As there is no possibility in the AQC to make single shot box car integration measurements it cannot be compared directly to the SSSv3. Therefore the means $S_{\text{FPGA}}(N)$ of the single shot measurements performed by the FPGA card with different integration times $t_N = N/f_s$ are compared to the sum $S_{\text{AQC}}(N)$ of the averaged measurement response

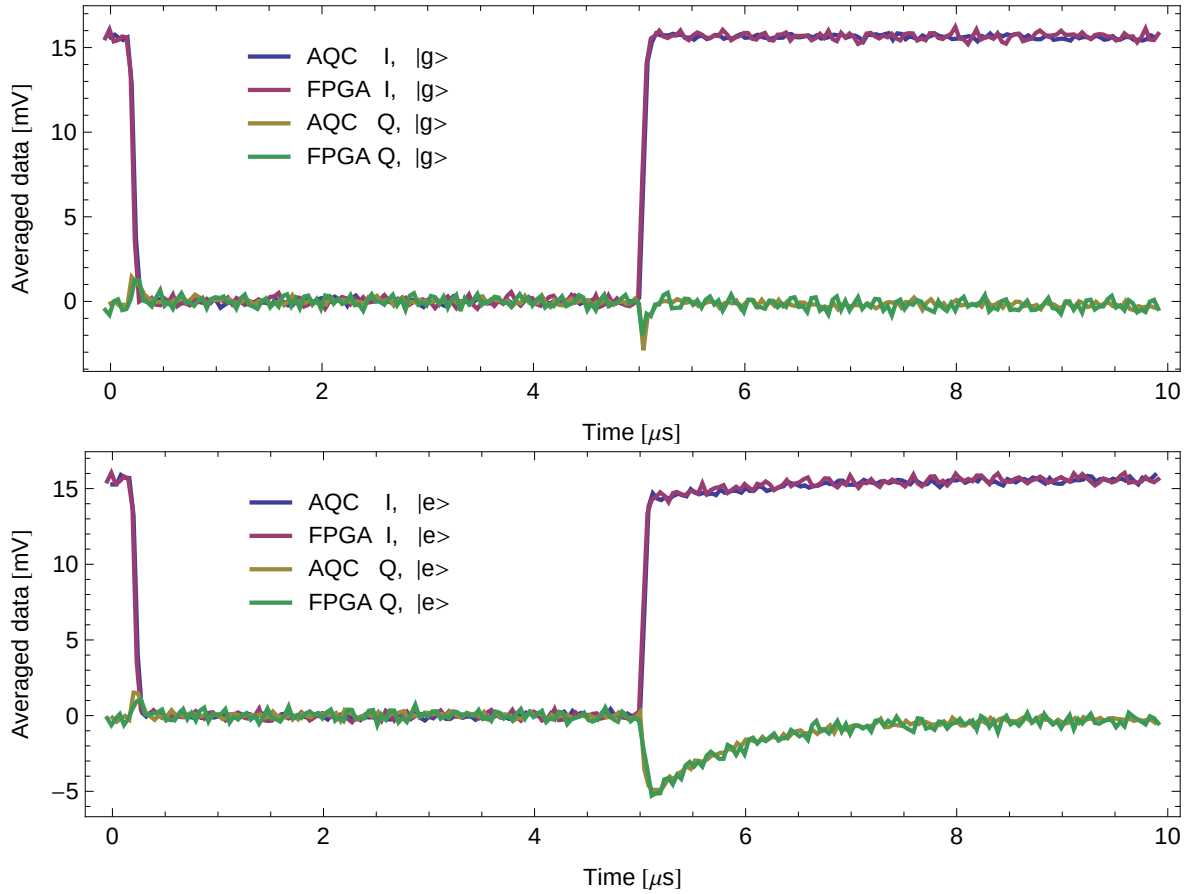


Figure 5.8: Comparison of averaged measurement response recorded with the AQC and the FPGA card respectively first with the qubit in the ground state $|g\rangle$ (top) and second with the qubit in the excited state $|e\rangle$ (bottom). Both data sets (AQC and FPGA) are rotated in the I-Q-plane to take grid of the different mixer arms angles, different propagation lengths and different trigger time points. There is no rotation applied between the two qubit states.

$a_{\mathrm{AQC}}(t_n)$ performed by the AQC. This is possible as (compare Equation (5.1))

$$\begin{aligned} S_{\mathrm{AQC}}(N) &= \sum_{n=0}^{N-1} a_{\mathrm{AQC}}(t_n) = \sum_{n=0}^{N-1} \left(\frac{1}{J} \sum_{j=0}^{J-1} \left(\frac{1}{n_{\mathrm{if}}} \sum_{n'=n-n_{\mathrm{if}}-1}^{n} x_j(t_{n'})\, e^{-i\cdot 2\pi\nu_{\mathrm{if}}\cdot t_{n'}} \right) \right) \\ &= \frac{1}{J} \sum_{j=0}^{J-1} \left(\sum_{n=0}^{N-1} \left(\frac{1}{n_{\mathrm{if}}} \sum_{n'=n-n_{\mathrm{if}}-1}^{n} x_j(t_{n'})\, e^{-i\cdot 2\pi\nu_{\mathrm{if}}\cdot t_{n'}} \right) \right) = \frac{1}{J} \sum_{j=0}^{J-1} s_j(N) \\ &= \frac{1}{J'} \sum_{j=0}^{J'-1} s_j(N) = S_{\mathrm{FPGA}}(N) \end{aligned}$$

where J is the number of averages of the AQC and J' the number of shots taken for the FPGA card. The comparison is shown Figure 5.9. The relatively larger noise of the FPGA SSSv3 data can be explained by the uncorrelated single shot box car integrations

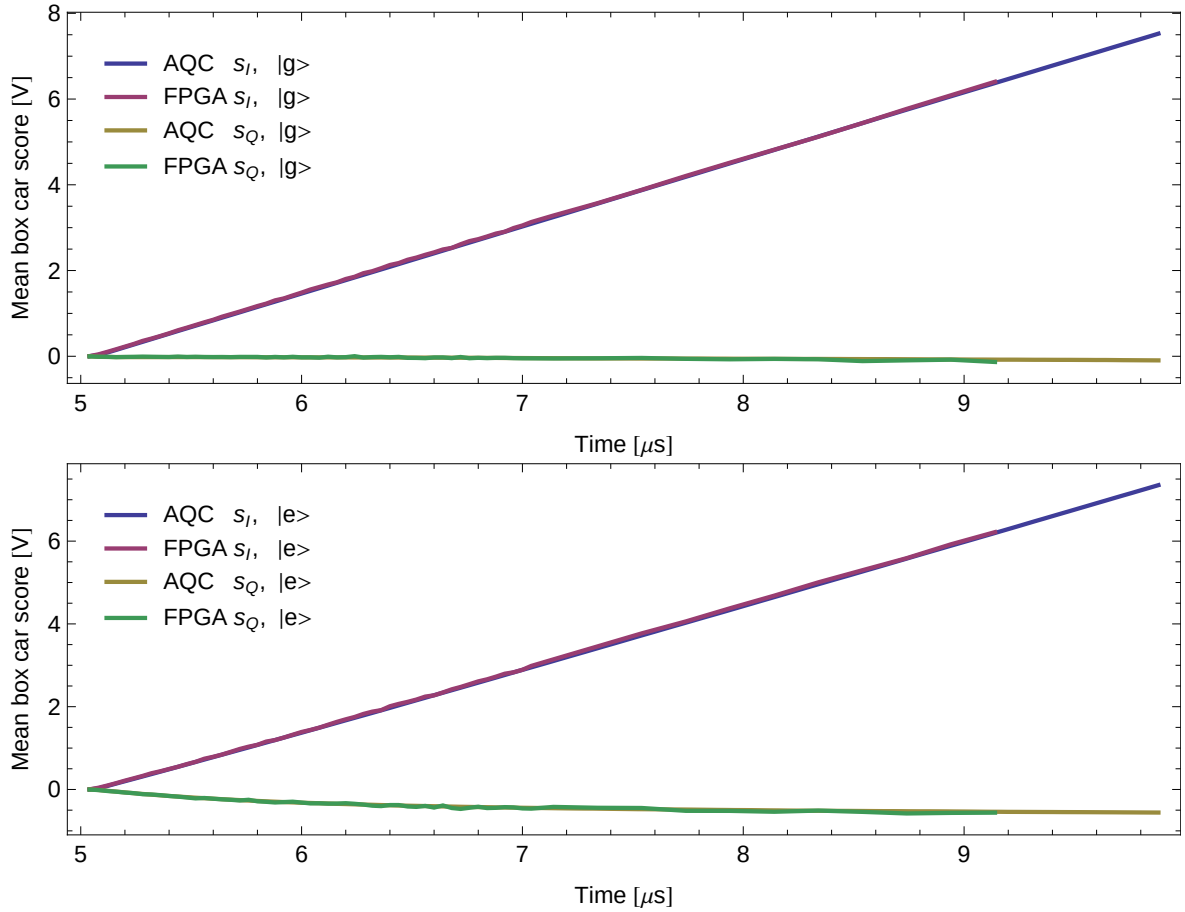


Figure 5.9: Comparison of the summed averaged measurement response recorded with the AQC and the single shot measurement (SSSv3) recorded with the FPGA card respectively. Top: with the qubit in the ground state $|g\rangle$. Bottom: with the qubit in the excited state $|e\rangle$. Both data sets (AQC and FPGA) are rotated in the I-Q-plane with the same angles as they were rotated in the comparison of the two averagers (Figure 5.8).

for the different integration time points t_N whereby the summed averaged AQC data is correlated.

Chapter 6

System noise

For being able to compare the performance of single shot measurements with the theoretically expected one we need to achieve a good understanding of the noise in the experimental system. More precisely the noise and signal power remaining after single shot integrations is needed. Therefore the integrated noise and signal power is discussed in Section 6.1 and 6.2 respectively. The subsequent section discusses theoretically the noise temperature which is a characteristic to describe quantitatively the noise generated by an amplifier as in our case. This discussion is followed by the measurement of the noise temperature and the overall gain of the amplifier chain needed to calculate out the noise temperature, see Section 6.4. The integrated signal to noise ratio as needed in the theory for single shot measurements is discussed and worked out in the last section.

6.1 Integrated noise power

System noise has a large influence on the measurement signal. The direct inspection of a single trace of a measurement signal is not very informative and therefore we need to achieve a good understanding to handle the noise. In this section I will analyse the noise power remaining after a box car integration with the SSSv3.

The main portion of noise is expected to be generated by the first cold amplifier in the measurement setup (Figure 3.3). It is white around the frequency of interest (Bianchetti, 2008). The frequency band is some tens of MHz broad and centred around the resonator frequency ν_{meas} which is frequently around 6.5 GHz. At room temperature the noise is amplified two times. Then it is mixed with a local oscillator (LO) with a frequency $\nu_{\mathrm{LO}} = \nu_{\mathrm{meas}} + \nu_{\mathrm{if}}$, where ν_{if} is in the order of some MHz. Typically ν_{if} is 10 MHz. For time resolved measurements it is 25 MHz. After the mixing the band of interest is around ν_{if} and still white. Now it is amplified a third time. In the next stage the white Gaussian noise is low pass filtered by a passive 30 MHz low pass filter, here by the SLP-30+ (Mini-Circuits, n.d.) with a -3 dB point slightly above 35 MHz. From this point the noise spectrum is not white any more but keeps its whiteness over a certain bandwidth $BW \approx 35$ MHz and we need to keep track of to interpret our data correctly. The spectrum enters the FPGA card to be digitised and digitally homodyned (downconverted and filtered to DC). The digital processing is discussed in detail in Section 4.4.1 and verified in Section 5.2. Schematically

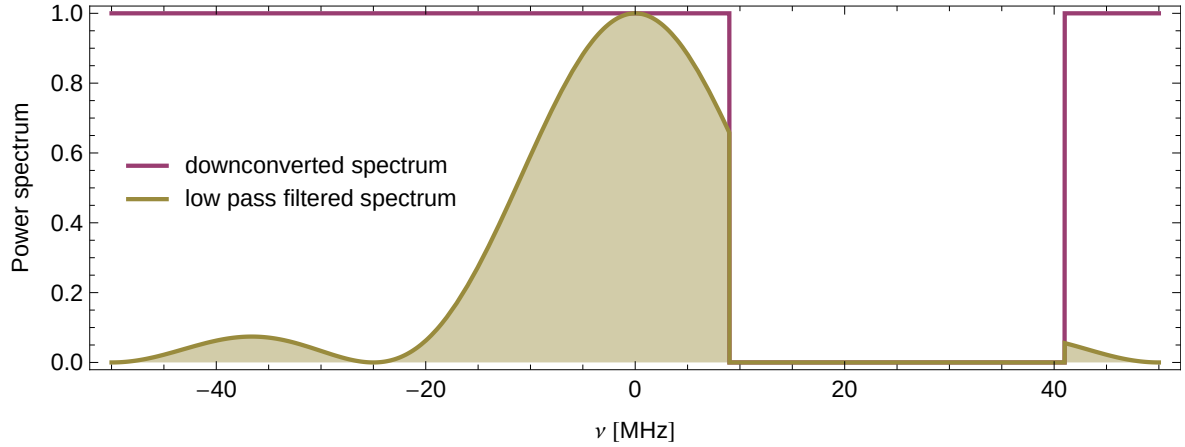


Figure 6.1: Schematic noise power spectrum in the DDCv3, see Section 4.4.1 for details. The downconverted spectrum (purple) is a left shifted (25 MHz) version of the spectrum (34 MHz low passed white noise) digitised by the FPGA card. The low pass filtered spectrum (ochre) is the spectrum of the data leaving the DDCv3 and entering the box car integration SSSv3. The total power in the remaining data is represented by the shaded area.

the ochre spectrum of Figure 6.1 results and leaves the DDCv3 of the FPGA. The total noise power is given by the integral over the noise spectrum, see the ochre shaded area in Figure 6.1.

For single shot measurements we are interested in the noise still present in the signal. The SSSv3 is the application in the FPGA responsible for the single shot box car integration. Since this application just sums up the signal leaving the DDCv3 it can be considered as a further filter step on these data performed by a convolution with a square window corresponding to the box car integration. In the frequency domain the convolution corresponds to a multiplication of the noise spectrum with the DTFT of the square window. The DTFT of this square window is much narrower than in Section 4.4.1 as the length of the sum is usually longer than the sum responsible for the downconversion filtering. Figure 6.2 shows the result of the multiplication for an example integration time of 0.5 μs. The bandwidth of the green spectrum is much narrower compared to the ochre spectrum that leaves the DDCv3. The total power covered by the noise in the signal is given by the integration of all the frequency components. The remaining total integrated noise power is represented by the green shaded area.

The measurable total integrated noise power of the single shot scores is given by the variance σ_s^2 for the scores s_j, $j = 1, \ldots, J$. An integration time of t_N results in $N = t_N \cdot f_s$ integration points in the SSSv3 and a integrated noise power of

$$P_n = \frac{\sigma_s^2}{R}, \tag{6.1}$$

where $R = 50\,\Omega$ due to the single ended configuration of the ADC input. The noise power spectral density which is basically represented by the height of the purple curve in

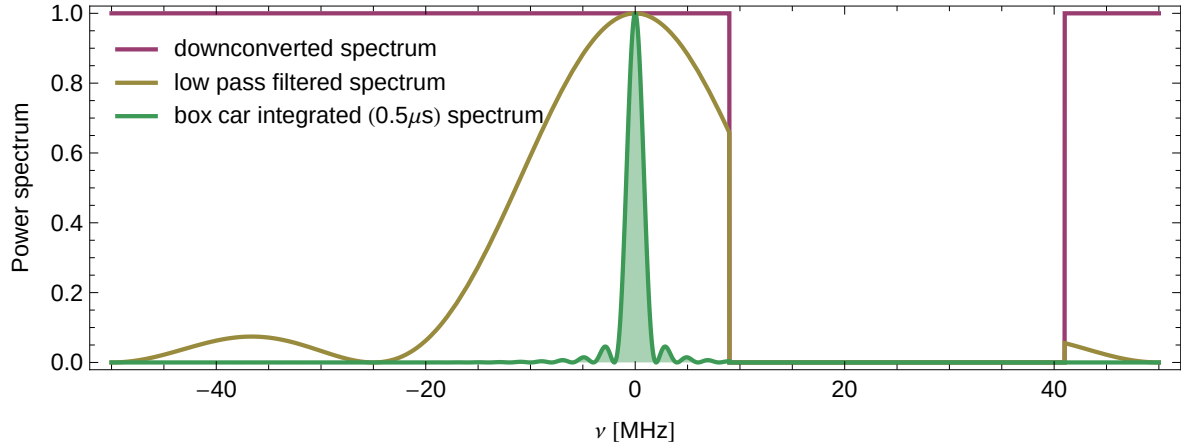


Figure 6.2: Schematic noise power spectrum in the DDCv3 and SSSv3. The downconverted spectrum (purple) and the low pass filtered spectrum (ochre) are the same as in Figure 6.1. The latter leaves the DDCv3 and enters the SSSv3. A multiplication of this ochre curve with the spectrum of a square window with the integration length results in the box car integrated (for 500 ns) spectrum (green). The spectrum is very narrow as a large amount of noise is filtered out. The remaining total noise power of the box car integrated signal is the shaded area which is the only observable property characterising the noise for the scores s_i saved by the the SSSv3.

Figure 6.2 can be derived from P_n, as shown in the next paragraph.

Using the commonly used definition in digital signal processing the DTFT for the data points $x(n)$ leaving the DDCv3 for different time points n is

$$X(m) = \sum_{n=0}^{L-1} x(n) e^{-2\pi i \frac{nm}{L}}, \tag{6.2}$$

where L is the length of the DTFT. The power spectrum of this DTFT is

$$|X(m)|^2$$

for each power bin with a resolution bandwidth of f_s/L. For a complex sinusoidal input $x(n)$ with amplitude A and a frequency $f_m = m\frac{f_s}{L}$ the magnitude $|X(m)|$ is $L \cdot A$ (Lyons, 2004). The power $|X(m)|^2$ in this bin with bandwidth f_s/L is $L^2 \cdot A^2$. However, as a noise input $x(n)$ consists in a superposition of many complex sinusoids with different amplitudes and phases the complex noise power spectral density is

$$S_n(m) = \frac{1}{\frac{f_s}{L} \cdot L^2} \cdot |X(m)|^2 \cdot \frac{1}{R}.$$

The total integrated power follows as

$$P_n = \frac{1}{R} \cdot \sum_{m=0}^{L-1} |X(m)|^2 = \sum_{m=0}^{L-1} L^2 \cdot \frac{f_s}{L} \cdot S_n(m). \tag{6.3}$$

In this equation the first sum over the power spectrum for a DTFT of a square window of length N is exactly $1/N$ in comparison to a completely flat spectrum with height $|X(0)|^2$ (compare Figure 6.2). Since the green spectrum in Figure 6.2 is not only the power spectrum of the square window but multiplied with the ochre spectrum the relation of $1/N$ only holds approximately. The next issue to keep into account is the bandwidth limited noise spectrum $BW = 34\,\text{MHz}$ in Figure 6.2. The ratio r_{filter} is the fraction of the area under the purple curve $(2 \cdot BW)$ relative to the green shaded area $(\approx f_s/N)$, so that

$$r_{\text{filter}} \approx \frac{2 \cdot BW}{f_s/N}.$$

A complex noise power spectral density $S_n(m)$ with the same form as the downconverted spectrum (purple line in Figure 6.2) is assumed. It has bandwidth BW but height S_n instead of 1. The measured integrated noise power P_n follows as

$$P_n = \frac{1}{r_{\text{filter}}} \cdot L^2 \cdot \sum_{m=0}^{L-1} \frac{f_s}{L} \cdot S_n(m) = \frac{L^2}{r_{\text{filter}}} \cdot \frac{f_s}{L} \cdot \left(\frac{2 \cdot BW}{f_s} \cdot L \right) \cdot S_n = \frac{2 \cdot BW \cdot L^2}{r_{\text{filter}}} \cdot S_n. \tag{6.4}$$

Using the approximate solution of r_{filter} and $L = N$, P_n simplifies to

$$P_n \approx L \cdot f_s \cdot S_n$$

where S_n already includes the $1/R$ factor. The height X_n^2 of the corresponding noise power spectrum $|X(m)|^2$ leads to

$$P_n \approx \frac{1}{R} \cdot X_n^2$$

where X_n^2 itself depends on the length of the box car integration sum and scales proportional to L. As consequence P_n grows linear with the integration length:

$$P_n \propto L.$$

6.2 Integrated signal power

To compare the signal with the integrated noise power the integrated signal power needs to be calculated. For a signal $x(n)$ and applying Equation (6.2) the signal power spectral density results as

$$S_s(m) = \frac{1}{\frac{f_s}{L} \cdot L^2} \cdot |X(m)|^2 \cdot \frac{1}{R}.$$

The total integrated signal power is

$$P_s = \frac{1}{R} \cdot \sum_{m=0}^{L-1} |X(m)|^2,$$

as in Section 6.1. Since most of the signal is in DC we assume a constant signal $x(n) = c$. In this case the Fourier spectrum is

$$X(m) = \begin{cases} Lc & m = 0, \\ 0 & m \neq 0, \end{cases}$$

and the integrated signal power

$$P_s = \frac{1}{R} \cdot |Lc|^2 = \frac{1}{R} \cdot L^2 \cdot |c|^2. \tag{6.5}$$

This is proportional to L^2

$$P_s \propto L^2.$$

As the signal is analog downconverted to ν_{if} before it is digitised, half of the signal power is filtered out digitally by the DDCv3 (see Section 4.4.1). So a digitised signal amplitude A_s results in $|c|^2 = {}^{A_s^2}/_2$ and the amplitude gets filtered to $|c| = {}^{A_s^2}/_{\sqrt{2}}$.

6.3 Noise temperature

The noise temperature of an amplifier is defined as the temperature of a resistor producing random voltages between its ends. The root mean squared voltage is given by Planck's black body radiation law as

$$V_{n,\text{rms}} = \sqrt{\frac{4h\nu \cdot BW}{e^{\frac{h\nu}{k_B T_n}} - 1} \cdot R},$$

where h is Planck's constant, k_B Boltzmann's constant, ν the frequency of interest with bandwidth BW, R the resistance of the resistor and T_n the noise temperature (Pozar, 1998). The amplifier is assumed to work perfectly without adding noise to the signal during the amplifying process. The only noise source is the "virtual" black body noise produced by the "virtual" resistor at the input of the amplifier. The noise power in the bandwidth BW is

$$P = \frac{V_{n,\text{rms}}^2}{4 \cdot R}.$$

For our frequency of interest $\nu \approx 6.5\,\text{GHz}$ and expected noise temperature $T_n \approx 4\,\text{K}$ it is an appropriate approximation to expand the exponential in $V_{n,\text{rms}}$ to first order. The

noise power density S defines the noise temperature as

$$S = \frac{1}{BW} \cdot P = k_B \cdot T_n, \tag{6.6}$$

where T_n is the noise temperature of the amplifier circuit. Measuring the noise power density S_o at the output of the amplifier the noise S at the input is amplified by G

$$S_o = G \cdot S$$

and the noise temperature can easily be calculated.

In our setup the signal passes the next amplifier at room temperature. This amplifier and the following ones do not add significant noise power to the signal. An amplifier at room temperature, that follows an cold amplifier, with a noise temperature $T_{n,2} = G \cdot T_n$ would add the same amount of noise to the signal as the proceeding one. As the amplification G from the cold amplifier to the next amplifier is in the order of 10^3 and the noise temperature $T_{n,2}$ of the latter one is around 43 K (Bianchetti, 2008) the noise added by this amplifier is less than $T_{n,2}/G \lessapprox 5\,\%$ in comparison to the amplified noise of the first amplifier. In comparison to the noise power already in the signal, the noise power added by the further following amplifiers is much smaller due to even higher amplified noise. Thus the noise temperature of the whole amplifying system is less than 5 % higher than the noise temperature T_n of the cold amplifier.

In the following sections I will focus on the whole amplifier system. The input of this big amplifier system is equal to the output of the resonator (a known signal source as explained in Section 6.4.1). Before the signal to be amplified reaches the input of the first cold amplifier (see Figure 3.3) it is damped by an unknown amount (cabling, connectors, circulators, ...). The damping factor only can be approximated with the damping of the components at room temperature to be in total $D \approx -7.9\,\mathrm{dB}$ (Bianchetti, 2008). This uncertainty of the damping makes it impossible to measure the cold amplifiers noise temperature accurately in the current measurement setup. The output of the big amplifier system is located at the ADCs of the data acquisition cards (AQC, FPGA card). To investigate the noise temperature of the system let S_s be the virtual system noise power density, T_n the corresponding system noise temperature and

$$S_g = G \cdot S_s$$

the amplified noise power density where G is the overall gain from the resonator output to the ADCs. The noise temperature $T_{n,1}$ of the first cold amplifier can be estimated to be

$$T_{n,1} \approx D \cdot T_n \tag{6.7}$$

once the system noise temperature T_n is measured. As the amplifier system includes an analog downconverter from the measurement frequency ν_{meas} to $\nu_{\mathrm{if}} = 10\,\mathrm{MHz}$ or $\nu_{\mathrm{if}} = 25\,\mathrm{MHz}$ including analog low pass filtering the noise power spectrum S_g is shifted in comparison to the system noise power spectrum S_s. Because of the analog low pass filter,

the spectrum S_g is only a very small region of the black body noise spectrum around the measurement frequency ν_{meas}. Anyhow, the low pass filtered spectrum is white around ν_{if} as Bianchetti (2008) had checked. The flatness over a wide frequency range of the black body noise spectrum before the analog downconversion was checked as well (Bianchetti, 2008).

6.4 Measurement of noise temperature

This section presents the measurement of the noise temperature of the amplifier chain. Beforehand various parameters need to be calculated in order to work out the noise temperature. A defined power source is necessary to measure the overall gain of the amplifier chain. This power source is experimentally calibrated by means of the AC-Stark shift of the qubit transition frequency (compare Section 2.3) in Section 6.4.1. The consecutive section describes the measurement performed to determine the noise temperature. In Section 6.4.3 the overall gain of the amplifier chain is worked out. The integrated noise power is then evaluated in Section 6.4.4 to be able to calculate the noise temperature in Section 6.4.5.

6.4.1 Calibration

Unfortunately, the noise temperature cannot be measured directly. The main problem is that the overall gain of a signal leaving the resonator to the ADCs is not known exactly. To account for this an AC-Stark calibration is performed. The theory for the qubits (Cooper pair box and transmon) predicts a change of the qubit transition frequency depending on the number of photons $\langle n \rangle$ that is on average in the resonator (Schuster et al., 2005). In the first step the resonator frequency is investigated by means of a low power spectroscopic measurement of the resonator without any qubit drive. Depending on the measurement frequency the transmission of the microwave field through the resonator is analysed. From this measurement the exact cavity resonance frequency ν_{res} and the photon decay rate $\kappa/2\pi = 2\,\delta\nu$ can easily (with a Lorentzian fit where $\delta\nu$ is the half width half maximum (HWHM)) be extracted. In the next step the qubit transition frequency ν_a is probed at low power spectroscopically while shining light with frequency ν_{res} at different powers into the resonator. With an independently measured qubit state dependent resonator shift χ, it is expected that each photon in the resonator shifts the qubit transition frequency ν_a about 2χ. For linear decreasing powers of the ν_{res} field ν_a decreases linearly. By means of the zero power crossing point and the slope of the linear decreasing behaviour it can be concluded (without knowing the exact damping of the field from the source to the input of the resonator) which power on the source results in a specific number of photons $\langle n \rangle$ on average in the resonator. As long as the frequency of the source is resonant with ν_{res} a power of -28.47 dBm per photon on average in the resonator was measured for this measurement setup and this sample.

In addition, a spectroscopic resonator measurement for different measurement powers is

performed to make the AC-Stark calibration more flexible. For different measurement powers $P_{\nu_{\text{meas}}}$ the transmission power for different measurement frequencies ν_{meas} around the resonator ν_{res} is probed. For each $P_{\nu_{\text{meas}}}$ dataset a Lorentzian is fitted to get the resonators resonance frequency ν_{res} and characteristic width $\delta\nu$ (HWHM). The portion

$$\frac{1}{1+\frac{(\nu_{\text{meas}}-\nu_{\text{res}})^2}{(\delta\nu)^2}} \tag{6.8}$$

of the signal power is transmitted through the cavity. When measuring with $\nu_{\text{meas}} = \nu_{\text{res}}$ the whole signal is transmitted through the cavity. For a measurement frequency of $\nu_{\text{meas}} = \nu_{\text{res}} \pm \delta\nu$ only half of the signal power is transmitted through the cavity, the other half is reflected to the source.

The AC-Stark calibration provides a known tunable signal source in the inner of the cryostat. The photon power P_γ at the resonator output for a given averaged photon number $\langle n \rangle$ in the resonator is given by

$$P_\gamma = \langle n \rangle \cdot h\nu \cdot \frac{\kappa}{2}, \tag{6.9}$$

where ν is the frequency of the photons in the resonator and κ the photon decay rate (Blais et al., 2004; Walls and Milburn, 2008). Equation (6.9) is valid for equal mirrors on both ends of the cavity. The photon decay rate can be extracted from the width $\delta\nu$ (HWHM) of the resonator measurement to $\kappa/2\pi = 2\,\delta\nu$. Together with the previous measurement the signal power leaving the resonator for different measurement frequencies ν_{meas} (not only for $\nu_{\text{meas}} = \nu_{\text{res}}$) can be calculated.

6.4.2 Measurement

The system noise temperature T_n is measured with the single shot application SSSv3 running on the FPGA card. There are two unknown parameters necessary to calculate T_n: the overall gain G and the system noise power density S_s. To determine G a specified signal is injected into the input of the amplifier system. A microwave of frequency ν_{meas} and power $P_{\nu_{\text{meas}}}$ is shone continuously into the cryostat to the resonator. The output of the resonator then provides a known signal power due to the AC-Stark calibration. This procedure is repeated for different measurement powers $P_{\nu_{\text{meas},k}}$. The resulting signals can then be used to get a more accurate estimate when calculating G. For each $P_{\nu_{\text{meas},k}}$ 10 000 single shot scores s_j with eight different integration times $N_i = \{10, 30, \ldots, 150\}$ are measured applying a shot repetition rate of $1/20\,\mu\text{s}$. The use of different integration times is necessary to verify that the result does not depend on the box car integration filter and that the filter is well understood.

Since the amplifier system always adds noise to the signal the unknown parameter S_s is automatically measured together with the gain measurement. In the analysis of the measurement data the mean of the single shot scores s_j will determine the signal power and therefore the gain G. In addition the variance of the s_j specifies the noise power

density S_g and therefore the system noise power density S_s.

6.4.3 Integrated signal power – overall gain

The integrated signal power $P_{s,k}$ for a constant signal c_k is

$$P_{s,k} = \frac{L^2 \cdot |c_k|^2}{R},$$

compare Equation (6.5). The SSSv3 sums up $L = N_i$ times the signal c. Therefore the mean $\langle s_j \rangle$ of the scores s_j is equal to

$$\langle s_j \rangle = L \cdot c.$$

The amplified (not integrated) signal power $P_{g,k}$ before digitising accounting that half of the signal power is filtered out by the DDCv3 (see Section 6.2) is

$$P_{g,k} = \frac{1}{R} \cdot 2|c_k|^2 = \frac{1}{R} \cdot \frac{2|\langle s_j \rangle_{i,k}|^2}{N_i^2}$$

and the signal power $P_{\gamma,k}$ at the input of the amplifier system

$$P_{\gamma,k} = \frac{1}{G} \cdot P_{g,k}.$$

The power at the output of the resonator is linear in the average photon number $\langle n \rangle$, compare Equation (6.9). The amplitude of the signal per photon in the resonator can be calculated to:

$$|c(\langle n \rangle)| = \sqrt{\tfrac{1}{2} \cdot R \cdot P_g} = \sqrt{\tfrac{1}{2} \cdot R \cdot G \cdot P_\gamma} = \sqrt{\tfrac{1}{2} \cdot R \cdot G \cdot \langle n \rangle \cdot h\nu \cdot \frac{\kappa}{2}}.$$

Therefore the mean amplitude squared can be fitted to a line via a linear regression with

$$|\langle s_j \rangle_i (\langle n \rangle)|^2 = N_i^2 \cdot |c(\langle n \rangle)|^2 = N_i^2 \cdot \tfrac{1}{2} \cdot R \cdot G \cdot \langle n \rangle \cdot h\nu \cdot \frac{\kappa}{2}, \tag{6.10}$$

where each measurement power $P_{\nu_{\mathrm{meas},k}}$ is replaced with the average photon number $\langle n \rangle$. Figure 6.3 confirms the square behaviour in the integration time, where the $|\langle s_j \rangle_i (\langle n \rangle)|^2$ is shown for a fixed measurement power $\langle n \rangle$ and is divided by $R = 50\,\Omega$ to get the integrated signal power. To further improve the fit, the right hand side of Equation (6.10) is corrected with the transmission factor calculated in Equation (6.8). This correction is never below 0.99 for all measurement powers included in the fit, as the measurement was performed very accurately with $\nu_{\mathrm{meas}} = \nu_{\mathrm{res}}$. Figure 6.4 confirms the linear dependence in the measurement power $\langle n \rangle$ expected from Equation (6.10). In the fit high measurement powers were neglected as there are deviations to the expected dependence visible. The

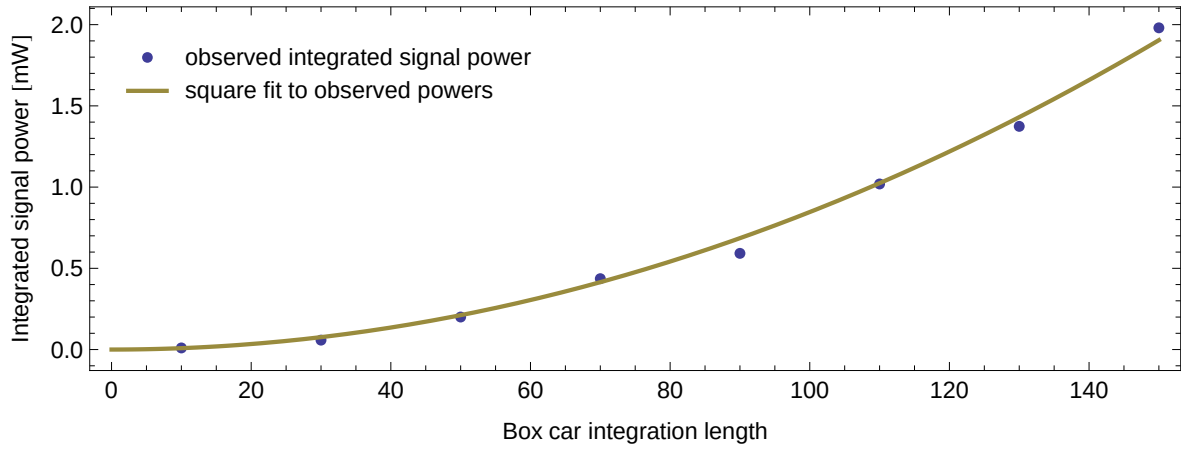


Figure 6.3: Integrated signal power $P_s = |\langle s_j \rangle|^2/R$ for different box car integration points. The experimental observed integrated signal powers (blue dotted) show good square behaviour in the integration time N_i as expected in Equation (6.10) and represented by the fit to the observed powers (ochre line).

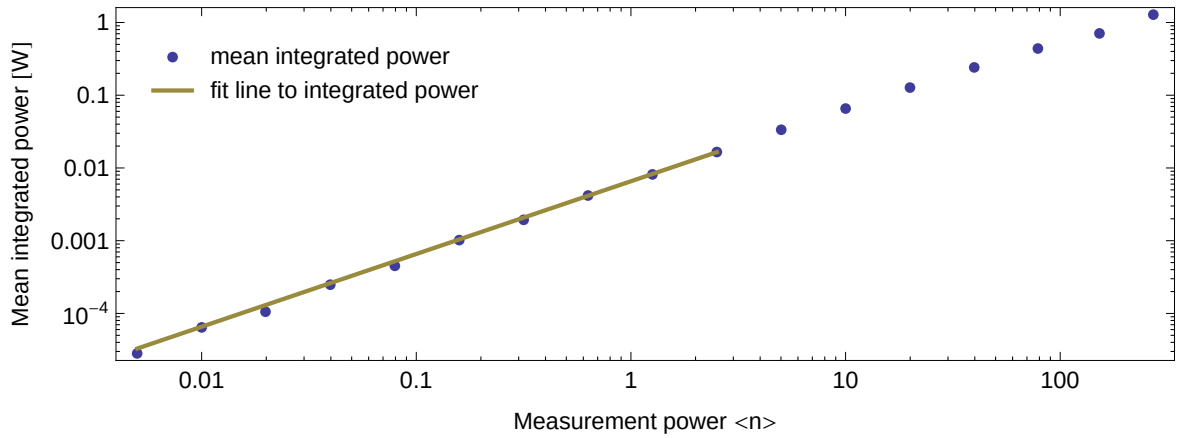


Figure 6.4: Integrated signal power $P_s = |\langle s_j \rangle|^2/R$ for different measurement powers $\langle n \rangle$. The experimental observed integrated signal powers (blue dotted) go linear with the measurement power $\langle n \rangle$, compare linear fit to the data (ochre line).

resulting fit to the observed integrated signal power

$$P_s(\langle n \rangle) = \frac{|\langle s_j \rangle_i (\langle n \rangle)|^2}{R} = N_i^2 \cdot \tfrac{1}{2} \cdot G \cdot \langle n \rangle \cdot h\nu \cdot \frac{\kappa}{2}$$

allows to calculate the total gain G for the known parameters ν_{meas}, κ and R for a single box car integration length $N_i = 110$ to $G \approx 98\,\text{dB}$.

6.4.4 Integrated noise power – noise power density

The integrated noise power P_n is constant for all measurement powers as it is independently generated by the amplifier system. The noise power spectral density $S_n(\nu)$ has the form assumed in Equation (6.4) with height S_n. The sum of the digitised noise is taken by the SSSv3 with L box car integration time points. Taking $J = 10\,000$ single shot integrations at very different times leads to a very high resolution in the frequency domain. A good approximation is achieved by neglecting deviations caused by noise in the mean $\langle s_j \rangle$ of the single shot scores s_j. The total integrated noise power remains equal even for the time delay between the single shot measurements so that the variance σ_s^2 of the s_j, $j = 1, \ldots, 10\,000$, is

$$\sigma_s^2 = \sum_{m=0}^{L-1} |X(m)|^2$$

(see Equation (6.1) and (6.3)). Using Equation (6.4) the height of the noise power spectral density around ν_{if} at the ADC follows as

$$S_n = \frac{r_{\text{filter}}}{2 \cdot BW \cdot L^2} \cdot \frac{\sigma_s^2}{R}, \tag{6.11}$$

where the last factor, the integrated noise power $P_n = \sigma_s^2/R$ (see Equation (6.1)), is displayed in Figure 6.5. As expected P_n grows approximately linear with the box car integration length L. From P_n the height S_n of the noise power density that enters the ADC can be calculated with Equation (6.11), compare Figure 6.6. Comparing the line fit (linear regression) to the S_n with the mean of the S_n confirms that S_n is independent of the box car integration time as it is the power on the input of the ADC and not related to the digital data processing. The mean of the S_n is used to predict the integrated noise power for any arbitrary chosen integration time, compare the ochre line in Figure 6.5. The observed integrated noise powers P_n are well fitted by the line.

The stability of the S_n can be assessed in Figure 6.7 in which it is shown for different measurement powers. The noise power density S_n remains constant for measurement powers up to -18 dBm. At higher powers the signal has effects on the variance and therefore these powers were excluded in further calculations. The mean of the lowest ten measurement powers corresponds to the height of the noise power spectral density around ν_{if} at the input of the ADC: $S_n = (1.77 \pm 0.01)^{\text{pW}}/_{\text{Hz}}$ in the case of $\nu_{\text{if}} = 25\,\text{MHz}$ and $S_n = (1.91 \pm 0.01)^{\text{pW}}/_{\text{Hz}}$ in the case of $\nu_{\text{if}} = 10\,\text{MHz}$. The larger noise density for

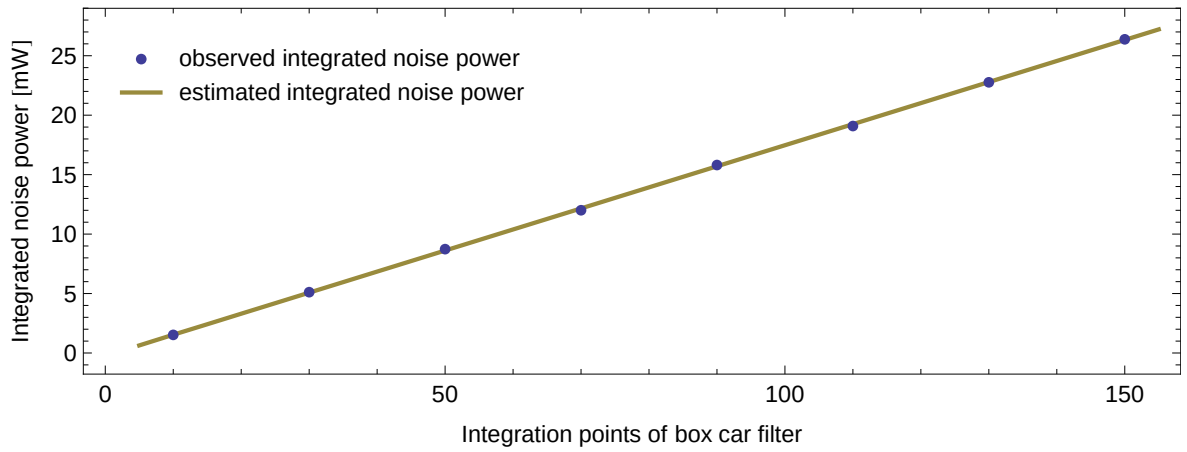


Figure 6.5: Integrated noise power $P_n = \sigma_s^2/R$ (Equation (6.1)) for different box car integration points. The experimental observed integrated noise powers (blue) show approximately linear behaviour in the integration time. From these data the integrated noise power for any arbitrary box car integration point number can be estimated (ochre). The measurement was performed in the "Vericold" cryostat of our laboratory at a measurement power of -33 dBm and $\nu_{\text{if}} = 25\,\text{MHz}$.

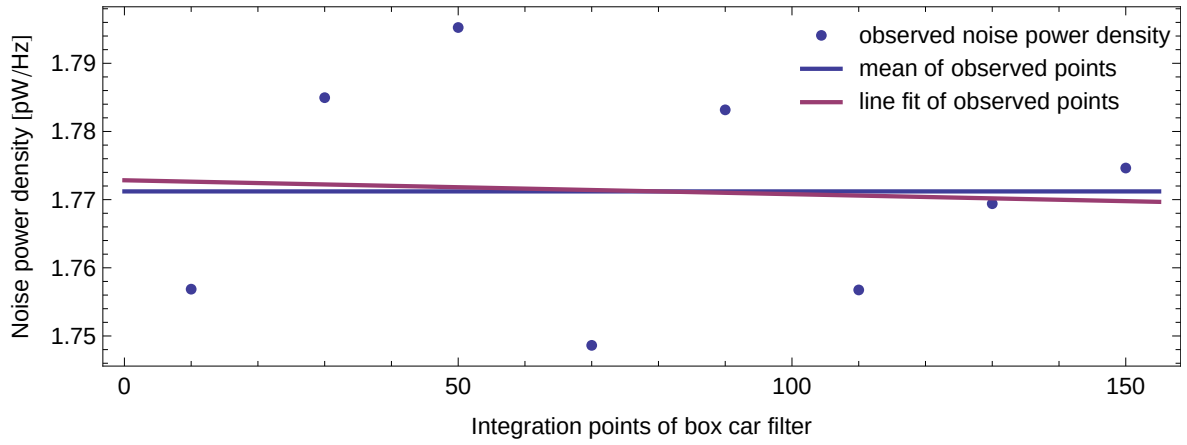


Figure 6.6: Height of noise power spectral density S_n. The observed noise power density (blue dotted) is calculated through the experimentally observed variance σ_s^2. To take into account different box car integration point numbers a line (purple) is fitted to the S_n via linear regression. The mean of the observed S_n (blue line) is a good approximation to the line confirming the expected behaviour which should not depend on the integration time. The measurement was performed in our "Vericold" cryostat at a measurement power of -33 dBm and $\nu_{\text{if}} = 25\,\text{MHz}$.

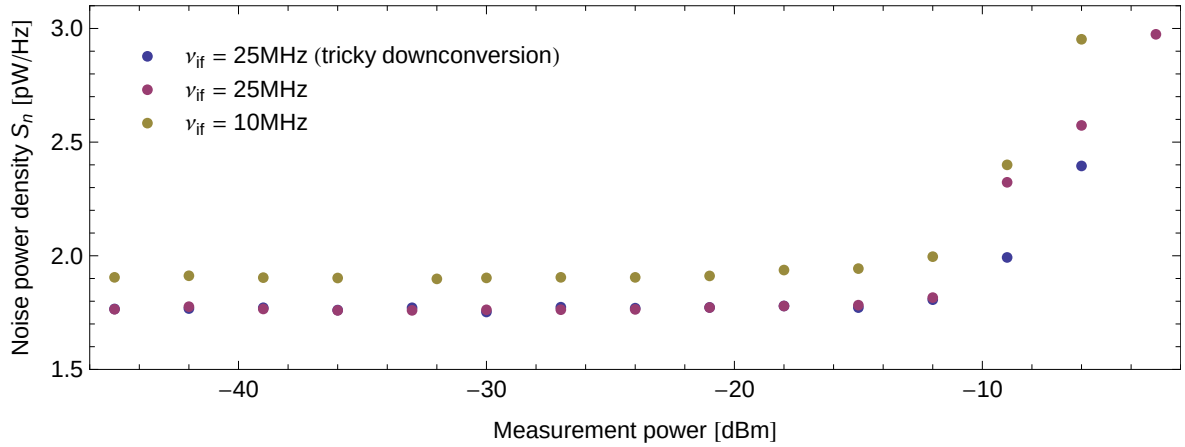


Figure 6.7: Height of the noise power spectral density S_n for different measurement powers. The measurement was performed in our "Vericold" cryostat for different ν_{if} and different channels of the DDCv3. Blue: tricky downconversion for $\nu_{\text{if}} = 25\,\text{MHz}$ without requiring any multiplication (see Section 4.4.1), purple: standard downconversion for $\nu_{\text{if}} = 25\,\text{MHz}$, ochre: standard downconversion for $\nu_{\text{if}} = 10\,\text{MHz}$. The noise power density S_n remains constant for powers up to -18 dBm. Higher powered signals have effects on the variance and are excluded in further calculations. The larger noise density for $\nu_{\text{if}} = 10\,\text{MHz}$ indicates a larger amplification than for $\nu_{\text{if}} = 25\,\text{MHz}$.

$\nu_{\text{if}} = 10\,\text{MHz}$ indicates a 0.05 dB larger amplification. With the noise power density S_n the integrated noise power can directly be calculated and therefore also the variance of the single shots σ_s^2 caused by noise for any arbitrary integration point number L:

$$P_n = \frac{\sigma_s^2}{R} = \frac{2 \cdot BW \cdot L^2}{r_{\text{filter}}} \cdot S_n,$$

compare Equation (6.11).

6.4.5 Noise temperature

Since all unknown parameters are measured we can calculate the system noise temperature. As described in Section 6.4.3 the gain is

$$G_i = \frac{2 \cdot |\langle s_j \rangle_i|^2}{R \cdot N_i^2 \cdot h\nu \cdot \frac{\kappa}{2}}$$

for the different box car integration lengths N_i. The noise power density at the ADC has a height of

$$S_{n,i} = \frac{r_{\text{filter}}}{2 \cdot BW \cdot N_i^2} \cdot \frac{\sigma_s^2}{R},$$

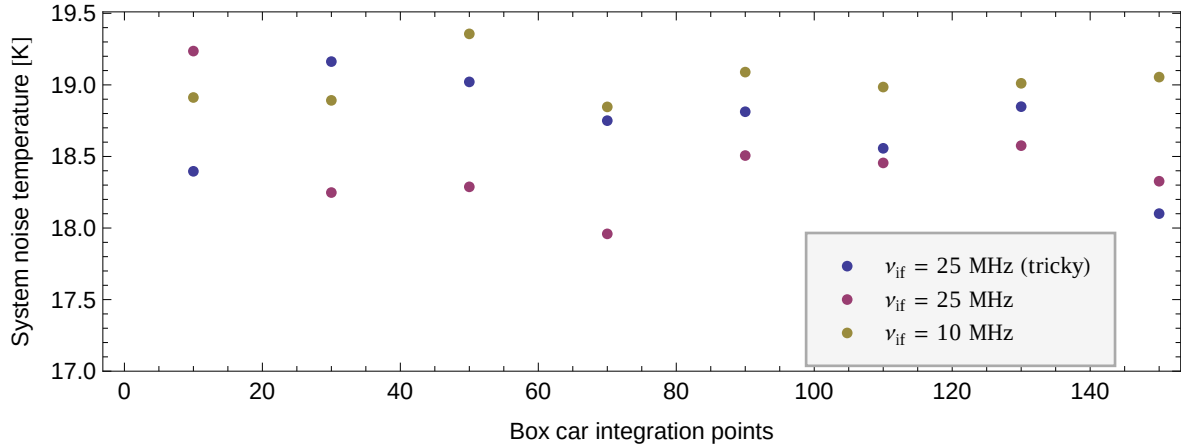


Figure 6.8: System noise temperature calculated at different box car integration times and different channels in the DDCv3. Blue: tricky downconversion for $\nu_{if} = 25\,\text{MHz}$ where no multiplication is necessary (see Section 4.4.1), purple: normal downconversion for $\nu_{if} = 25\,\text{MHz}$, ochre: normal downconversion for $\nu_{if} = 10\,\text{MHz}$. The temperature does not depend on the integration time and on ν_{if} indicating that these properties are respected correctly.

compare Equation (6.11). The virtual system noise power density is

$$S_{s,i} = \frac{1}{G} \cdot S_{n,i}$$

and the system noise temperature T_n is

$$T_n = \frac{1}{k_B} \cdot S_{s,i} = \frac{1}{k_B} \cdot \frac{S_{n,i}}{G} = \frac{h\nu \cdot \frac{\kappa}{2}}{k_B} \cdot \frac{r_{\text{filter}}}{2 \cdot BW} \cdot \frac{\sigma_{s,i}^2}{2|\langle s_j \rangle_i|^2} \approx \frac{h\nu \cdot \frac{\kappa}{2}}{k_B} \cdot \frac{N_i}{f_s} \cdot \frac{\sigma_{s,i}^2}{2|\langle s_j \rangle_i|^2}, \quad (6.12)$$

compare Equation (6.6). The overall gain and the system noise temperature is calculated for all different box car integration point numbers $N_i = 10, 30, \ldots, 150$ and for the three different channels in the DDCv3. Figure 6.8 shows the system noise temperature T_n whereby $T_n \approx (18.7 \pm 2.5)\,\text{K}$. The overall gain is calculated to be $G \approx (^{98.4}_{98.6} \pm 0.7)\,\text{dB}$ for $\nu_{if} = 25\,\text{MHz}$ (top) and $\nu_{if} = 10\,\text{MHz}$ (bottom) respectively. The higher gain of the lower ν_{if} already was expected due to the higher noise power spectral density observed in Figure 6.7. The noise temperature of the first cold amplifier can be estimated with Equation (6.7) to be around $T_{n,1} = (4.5 \pm 2.2)\,\text{K}$ with an estimated room temperature damping factor of $D = (-6.2 \pm 2)\,\text{dB}$.

The error was estimated by propagation of uncertainty. In the case of the system noise temperature T_n (compare Equation (6.12)) the error δ_{T_n} is

$$\delta_{T_n} = \sqrt{(\partial_\nu T_n \cdot \delta_\nu)^2 + (\partial_\kappa T_n \cdot \delta_\kappa)^2 + (\partial_{r_{\text{filter}}} T_n \cdot \delta_{r_{\text{filter}}})^2 + (\partial_{\sigma_s^2} T_n \cdot \delta_{\sigma_s^2})^2 + (\partial_{\langle s_j \rangle} T_n \cdot \delta_{\langle s_j \rangle})^2}$$

where $\partial_x T_n$ denotes the derivative of T_n with respect to the variable x and δ_x denotes the standard error in the variable x. As the AC-Stark calibration has the same dependency as

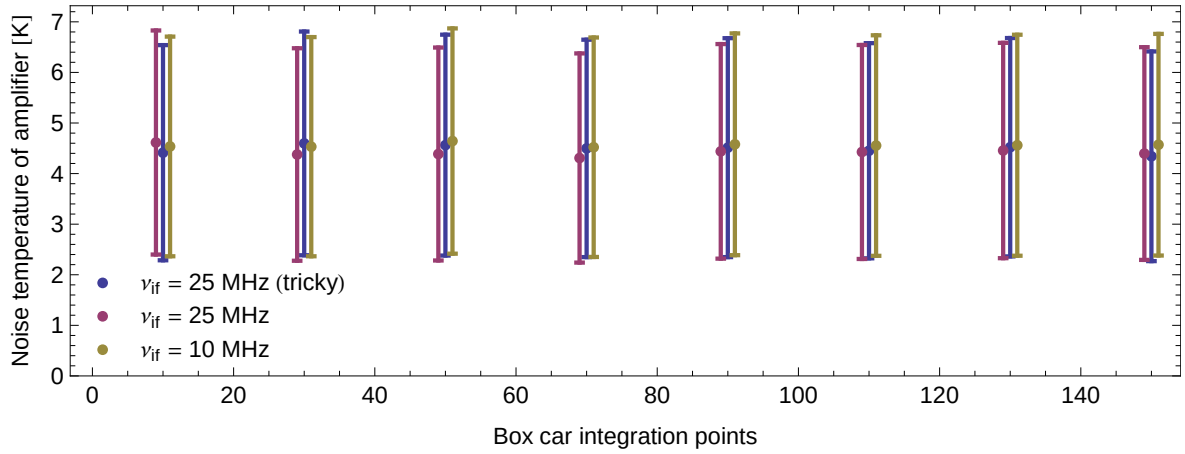


Figure 6.9: Noise temperature of the first cold amplifier calculated at different box car integration times and different channels in the DDCv3. Blue: tricky downconversion for $\nu_{\text{if}} = 25\,\text{MHz}$ where no multiplication is necessary (see Section 4.4.1), purple: normal downconversion for $\nu_{\text{if}} = 25\,\text{MHz}$, ochre: normal downconversion for $\nu_{\text{if}} = 10\,\text{MHz}$. To increase the visibility the three DDCv3 channels are shifted by one to the left and to the right respectively. All points lie within the error bars. There are no outliers.

the variable $\langle s_j \rangle$ this error was included in the transformation $\delta_{\langle s_j \rangle} \rightarrow \delta_{\langle s_j \rangle} + \langle s_j \rangle \cdot \delta_{\text{AC-Stark}}$ dominating over the bare $\delta_{\langle s_j \rangle}$ from the power fit. The error of the filter bandwidth BW is only included in the non trivial part of r_{filter} because the factor $2 \cdot BW$ cancels out in Equation (6.12). Analysing the different contributions to the uncertainty it results that the main uncertainty is caused by the $\delta_{\text{AC-Stark}}$. The error δ_κ contributes a factor of $1/50$ weaker than $\delta_{\text{AC-Stark}}$ to $\delta^2_{T_n}$. The same applies for the uncertainty δ_G in the gain. Analogously the noise temperature of the first cold amplifier $T_{n,1}$ can be estimated, see Figure 6.9. Here the largest contribution to the uncertainty is the uncertainty of the damping factor D from the output of the resonator up to the input of the cold amplifier. The contribution of δ_D to $\delta^2_{T_{n,1}}$ is a factor of 10 higher than the contribution of $\delta_{\text{AC-Stark}}$.

To conclude the measurement of the system noise temperature the number of noisy photons n_n that are added to the signal is calculated:

$$n_n = \frac{S_s \cdot BW}{h\nu \cdot BW} = \frac{k_B T_n}{h\nu} \approx 59 \pm 8.$$

6.5 Integrated signal to noise ratio

A different issue is to calculate how strong the noise is when trying to differentiate two measurement responses (e.g. between qubit in the ground state $|g\rangle$ and qubit in the excited state $|e\rangle$). This is to be done by the SSSv3 (taking scores $s_{|g\rangle,j}$ for $|g\rangle$ and $s_{|e\rangle,j}$ for $|e\rangle$) and is investigated in Chapter 7. To predict how separate the probability distributions for $s_{|g\rangle}$ and $s_{|e\rangle}$ are (they overlap due to the noise), the ratio r_{sn} of the integrated signal power to the integrated noise power achieved after integrating for the qubit relaxation time T_1

plays an important role, see Gambetta et al. (2007) and Chapter 7. The integrated signal to noise ratio r_{sn} is

$$r_{\mathrm{sn}} = \frac{P_s}{P_n} \tag{6.13}$$

where P_n is the integrated (over time T_1) noise power and P_s the integrated (over time T_1) signal power. P_n is calculated exactly as in Section 6.4.4 with $N = T_1 \cdot f_s$ integration points. The probability distributions for the ground state $|g\rangle$ shown in Figure 7.2 are exact Gaussian distributions with variance $\sigma^2 = \sqrt{\tau_f / r_{\mathrm{sn}}}$ where $\tau_f = T_f / T_1$ is the normalised integration time and the scores $s_{|g\rangle}$ are integrated over a time T_f.

The integrated signal power P_s now differs from the definition in Section 6.4.3 as we are not interested in the physical electric power but in the "information power" in order to discriminate the two measurement responses. There is only a small information gain when the measurement responses for $|g\rangle$ and $|e\rangle$ are similar even if they have high electrical power. Performing single shot measurements we are not interested in the averaged (over different decay times τ_d of the qubit changing from state $|e\rangle$ to $|g\rangle$) measurement response but in the measurement response for a well defined qubit decay time $\tau_d > 1$, e.g. $\tau_d = \infty$ shown in Figure 3.5. The signal power to gain information of a qubit state is the difference between the $|g\rangle$ and $|e\rangle$ measurement response, compare the green line in Figure 3.5. As described in Section 6.2 the integrated signal power P_s is calculated but with the signal $x(t_n) = \Delta I(t_n) + i \cdot \Delta Q(t_n)$ where $\Delta I(t_n)$ and $\Delta Q(t_n)$ are the difference quadratures of the measurement response for a non decaying qubit (green line in Figure 3.5). The single shot integration of the SSSv3 begins at time $\tau = 0$ (compare Figure 3.5) and ends at time $\tau = 1$, so that

$$s_j = \sum_{n=0}^{N-1} x(t_n),$$

calculating the mean of $x(t_n), n = 0, \ldots, N-1$ times N. Except for the settling time that scales inverse with the photon decay rate κ, $x(t_n)$ is constant. The larger κ is the faster raises the measurement response after switching on the measurement signal and the better is the approximation for a constant $x(t_n) = c$. The integrated signal power follows as

$$P_s = \frac{1}{R} \cdot N^2 \cdot |c|^2.$$

To compute P_s exactly, the DTFT $X(f_m)$ of the signal $x(t_n)$ is calculated and multiplied with the DTFT $K(\nu)$ of the square window with length T_1, compare Figure 4.8 for example power spectra $|K(\nu)|^2$. Here there is no need to additionally multiply with the DDCv3 spectrum as the data that is fitted by the cavity Bloch equations already passed the digital downconversion. For the same reason as in Section 6.2 the signal amplitude needs not to be scaled with $1/\sqrt{2}$. An example of the power spectrum $|X(f_m)|^2/R$ is shown in Figure 6.10. The exact total integrated signal power is

$$P_s = \frac{1}{R} \cdot \sum_{m=0}^{N-1} |X(f_m)|^2 \cdot |K(f_m)|^2.$$

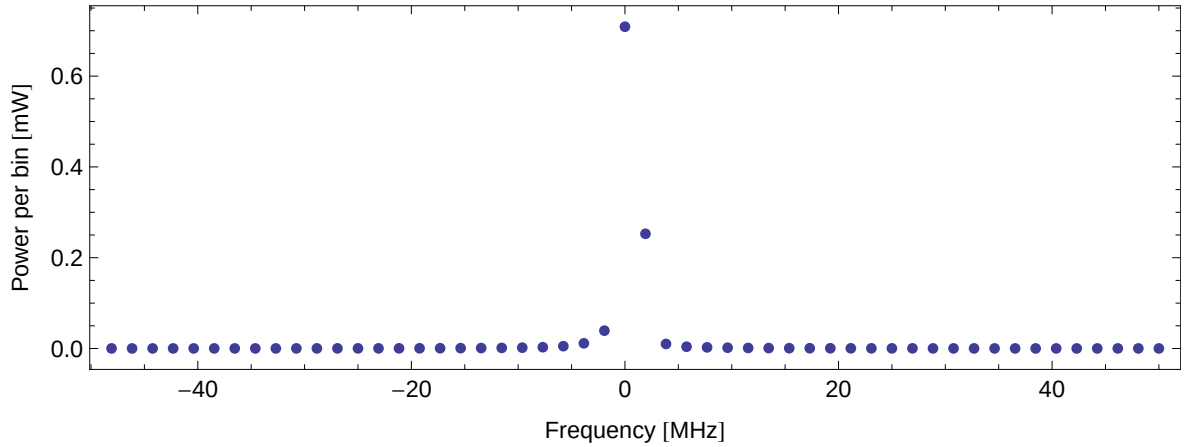


Figure 6.10: Power spectrum $|X(f_m)|^2/R$ for the difference signal of a cavity Bloch fit at measurement frequency $\nu_{\text{meas}} = 6.44564\,\text{GHz}$.

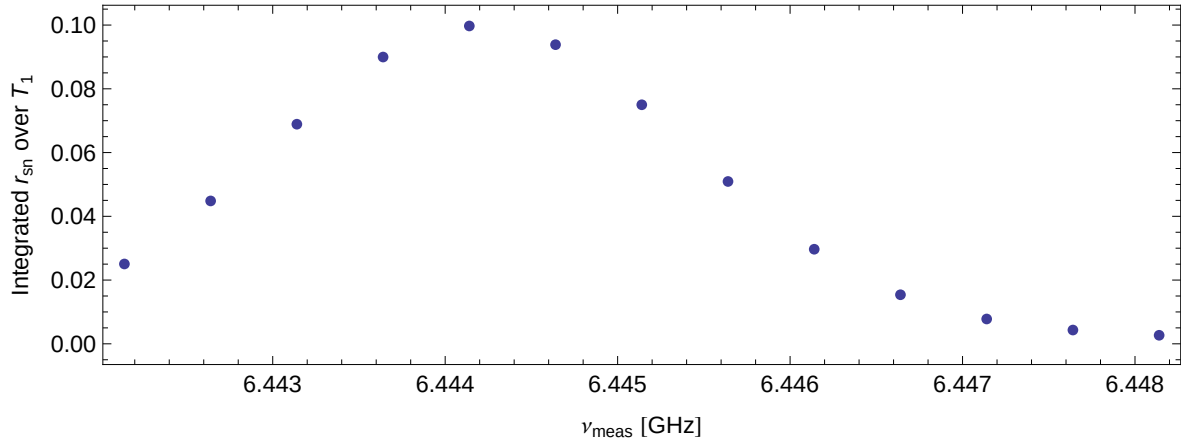


Figure 6.11: Integrated signal to noise ratio r_{sn} calculated using a fit to the cavity Bloch equations at different measurement frequencies ν_{meas}. The measurement response was adjusted to represent the single shot measurement response for the case of a non decaying qubit.

Most of the signal power that is not around 0 MHz is filtered out by the box car integration filter $K(\nu)$ as long as the qubit lifetime T_1 is sufficiently long.

P_n is computed using Equation (6.4) and the corresponding measurements of S_n as in Section 6.4.4, so that now the integrated signal to noise ratio r_{sn} can be calculated. As a note, an increasing qubit life time T_1 increases r_{sn} on a linear scale:

$$r_{\text{sn}} = \frac{P_s}{P_n} \propto \frac{N^2}{N} = N.$$

Figure 6.11 shows the result for r_{sn} at the different measurement frequencies ν_{meas}. The cavity Bloch fit was performed as described in Section 3.3

Chapter 7

Single shot read-out

With the previous chapters all the prerequisites are in place for a detailed discussion on single shot read-out of qubit states. The first section discusses theoretically the single shot score, the outcome of the single shot measurement signal analysis. It is followed by a theoretical discussion of the read-out fidelity, a measure for the quality of the single shot read-out. This section is extended by Section 7.2.3 which introduces the strategy for the experimental calculation of the read-out fidelity. Section 7.3 then presents single shot measurements and compares the read-out performance with the theoretically expected one. In Section 7.4 a scheme to increase the read-out fidelity is elaborated. The consecutive section demonstrates a joint multi-qubit single shot read-out. The chapter closes with a high power single shot measurement where read-out fidelities up to 73 % were achieved.

7.1 Single shot score

In the single shot analysis a score s_j is calculated for each measurement shot j. Based on this score a guess is made whether the qubit was initially in the ground state $|g\rangle$ or in the excited state $|e\rangle$. However, there is no perfect measurement and therefore a suggestion is the only thing that can be done. The goal is therefore to improve this suggestion and to improve the score calculation in order to increase the read out fidelity. Gambetta et al. (2007) discussed the perfect single shot measurement protocol for an appropriate system. Here, the simplest measurement protocol, the box car integration, is investigated to assess its applicability.

As shown in Section 2.3 the resonance frequency shifts to $\nu_{\mathrm{res}} \pm \chi$ for qubit state $|e\rangle$ or $|g\rangle$ respectively. The resonator shift is assumed to occur instantaneously. The photons leaving the resonator immediately reflect the information of the qubit state. Since a pulsed measurement is performed no cavity raise time is assumed resulting in an instantaneous measurement response when switching on the measurement pulse with frequency ν_{res}. Based on these assumptions there is no information about the resonance frequency represented in the I-quadrature of the transmission but there is an around zero symmetric measurement response in the Q-quadrature, compare Figure 2.3. This quadrature normalised to one corresponds to the measurement response $x_j(t)$ assumed in Gambetta et al. (2007). Figure 7.1 shows an example detector output $x_{j,|e\rangle}(t)$ where the initial qubit

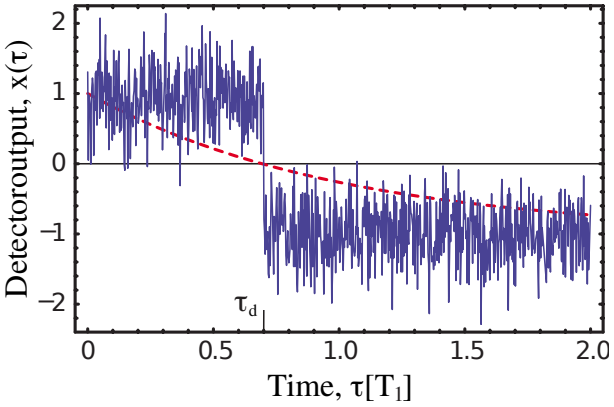


Figure 7.1: Assumed single shot detector output where the qubit decays from $|e\rangle$ to $|g\rangle$ at normalised time τ_d. To show the qubit decay in the noisy signal a high integrated signal to noise ratio of $r_{\mathrm{sn}} = 570$ is chosen. The red dashed line represents the signal averaged over many exponentially distributed qubit decay times (Gambetta et al., 2007).

state was $|e\rangle$. When measuring a qubit, which is initially in a complex superposition $a\,|g\rangle + b\,|e\rangle$ ($|a|^2 + |b|^2 = 1,\ a, b \in \mathbb{C}$), it collapses into the state $|g\rangle$ or $|e\rangle$ with probability $|a|^2$ or $|b|^2$ respectively, as quantum non demolition (QND) measurement is performed. The qubit remains then in its state leading to a constant measurement transmission until $|e\rangle$ decays spontaneously into $|g\rangle$. A spontaneous thermal excitation of the qubit from $|g\rangle$ to $|e\rangle$ is not assumed but can be caused by high measurement powers in the case in which qubit and resonator become entangled (Boissonneault et al., 2008). The time t is hereby normalised to $\tau = {}^{t}/_{T_1}$ (see Figure 7.1) where T_1 is the characteristic qubit life time.

In the box car integration the single shot measurement score s_j for each single shot j is defined as

$$s_j = \int_0^{\tau_f} x_j(\tau)\, d\tau = \sum_{n=0}^{N-1} x_j(t_n), \tag{7.1}$$

where the integral is a sum when integrating a time discrete signal. The integration starts at $t_0 = 0$ and goes to a specified $\tau_f = {}^{t_N}/_{T_1}$ chosen in the way that $N = \tau_f\, T_1\, f_s$ where f_s is the sample frequency of the detector. As defined in Equation (6.13) the signal is superimposed by noise of integrated strength $P_n = {}^{1}/_{r_{\mathrm{sn}}}$ because the power is normalised to one. When integrating over time τ_f the probability distribution for the qubit to be initially in the ground state is

$$P_{|g\rangle}(s) = \frac{1}{\sqrt{2\pi}\,\sigma}\, e^{-(s+\tau_f)^2/(2\,\sigma^2)}, \tag{7.2}$$

where $-\tau_f$ is the mean and $\sigma = \sqrt{{}^{\tau_f}/_{r_{\mathrm{sn}}}}$ the standard deviation of the purely Gaussian distribution (Gambetta et al., 2007). The linear scaling of σ^2 with τ_f agrees with the linear scaling in the integration length of the integrated noise power described in Section 6.1. The curves to the left of the centre in Figure 7.2 show $P_{|g\rangle}(s)$ for four different integration times τ_f.

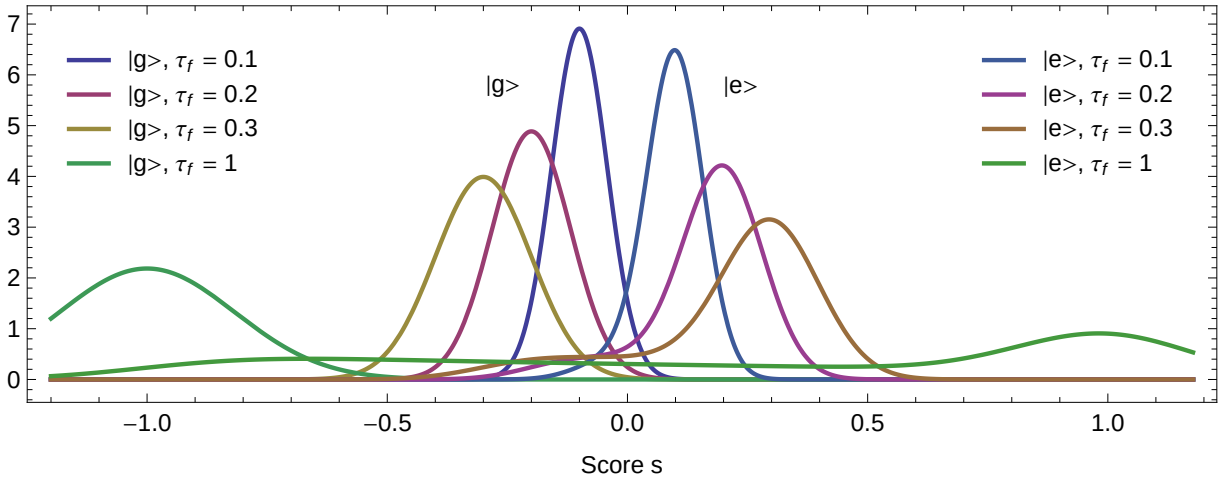


Figure 7.2: Probability distributions for score s with initial qubit state $|g\rangle$ or $|e\rangle$ for different integration times τ_f at a integrated signal to noise ratio $r_{\text{sn}} = 30$.

The probability distribution for the qubit to be initially in the excited state is slightly more complex as the qubit decays at random times. First the probability distribution for the score s is calculated when the qubit decays from $|e\rangle$ to $|g\rangle$ at time τ_d. When the qubit state lives longer than the integration lasts, $\tau_d > \tau_f$, the distribution is $P_{|g\rangle}(s)$, however with mean τ_f (first term in Equation (7.3)). If the qubit decays before the integration has finished, $\tau_d \leqslant \tau_f$, the mean is $\tau_d - (\tau_f - \tau_d) = 2\,\tau_d - \tau_f$ (second term in Equation (7.3)). Combining the two cases $P_{|e\rangle}(s|\tau_d)$ for a given decay time τ_d results in

$$P_{|e\rangle}(s|\tau_d) = \frac{1}{\sqrt{2\pi}\,\sigma}\, e^{-(s-\tau_f)^2/(2\,\sigma^2)}\,\theta(\tau_d - \tau_f) + \frac{1}{\sqrt{2\pi}\,\sigma}\, e^{-(s-(2\tau_d-\tau_f))^2/(2\,\sigma^2)}\,\theta(\tau_f - \tau_d), \quad (7.3)$$

where $\theta(\tau)$ is the Heaviside step function (Gambetta et al., 2007) controlling that only one of the two terms is included. The integration of all possible decay times τ exponentially weighted (as the decay times are exponentially distributed) leads to the score probability distribution given that the qubit initially was in state $|e\rangle$

$$P_{|e\rangle}(s) = \frac{1}{\sqrt{2\pi}\,\sigma}\, e^{-(s-\tau_f)^2/(2\,\sigma^2)-\tau_f} + \frac{1}{4}\, e^{-(s+\tau_f)/2+\sigma^2/8}\left[\text{erf}\left(\frac{\sigma^2-2(s-\tau_f)}{2\sqrt{2}\,\sigma}\right) - \text{erf}\left(\frac{\sigma^2-2(s+\tau_f)}{2\sqrt{2}\,\sigma}\right)\right] \quad (7.4)$$

(Gambetta et al., 2007) where $\text{erf}(z)$ is the error function defined as

$$\text{erf}(z) = \frac{2}{\sqrt{\pi}} \int_0^z e^{-t^2}\, dt.$$

The curves to the right of the centre in Figure 7.2 show $P_{|e\rangle}(s)$ for four different integration times. These distributions are not Gaussian any more. They have a Gaussian aspect for short integration times τ_f and deviate increasingly from this aspect for larger τ_f building up a tail pointing to the ground state distribution. The tail can be explained by the earlier decayed qubits because the early decayed score distribution (second term in

Equation (7.3)) is equal to $P_{|g\rangle}(s)$ (compare Equation (7.2)) for $\tau_f = 0$.

Experimentally the score is computed as in the discrete time sum version of Equation (7.1), however, the complex $x_j(t_n) = I_j(t_n) + i\,Q_j(t_n)$ quadrature signal is summed up resulting in a complex score s_j. As the signal is not normed to one all distributions are scaled in the way to keep their form and relative separation but not to change the theory. Unfortunately, the phase of the signal is randomly chosen at the beginning of the experiment so that the score distributions are rotated in the I-Q-plane even though all with the same phase. The computation of the single shot scores is done with the FPGA card using the SSSv3 application.

There is a second more advanced single shot score computation discussed in Gambetta et al. (2007)

$$s_j = \int_0^{\tau_f} k(\tau) \cdot x_j(\tau)\, d\tau = \sum_{n=0}^{N-1} k(t_n) \cdot x_j(t_n)$$

which can be solved numerically for an optimal linear filter kernel $k(t_n)$ for $\tau_f \to$ inf. This computation can be performed by the SSAv4 application running on the FPGA card. However, to find the optimal kernel more system parameter need to be known to design the optimal filter before the measurement (Gambetta et al., 2007). Before the application of this complicated procedure is used the simple box car integration done by SSSv3 is investigated and needs to be fully understood. It does not make much sense to complicate the measurement if the slight improvement of the read out fidelity is not absolutely essential.

7.2 Fidelity

7.2.1 Definition

The scores s_j are used to give a suggestion in which state the qubit was at the beginning of the single shot measurement. A threshold score ν_{th} is chosen. Every score $s_j < \nu_{\text{th}}$ indicates that the qubit was initially in the ground state $|g\rangle$ while every score $s_j > \nu_{\text{th}}$ indicates that the qubit was initially in the excited state $|e\rangle$. The read out fidelity F is then defined as one minus the percentage of falsely identified $|e\rangle$ minus the percentage of falsely identified $|g\rangle$:

$$F \equiv 1 - \int_{-\infty}^{\nu_{\text{th}}} P_{|e\rangle}(s)\, ds - \int_{\nu_{\text{th}}}^{\infty} P_{|g\rangle}(s)\, ds \tag{7.5}$$

(Gambetta et al., 2007). With this definition the fidelity is represented by one minus the two shaded areas in Figure 7.3. Moving the threshold ν_{th} to the left or to the right always reduces the fidelity as one of the areas increases faster than the other decreases. As consequence the optimal threshold is given by the cutting point of the two probability distributions given that both gradients have different signs in this point. For two identical

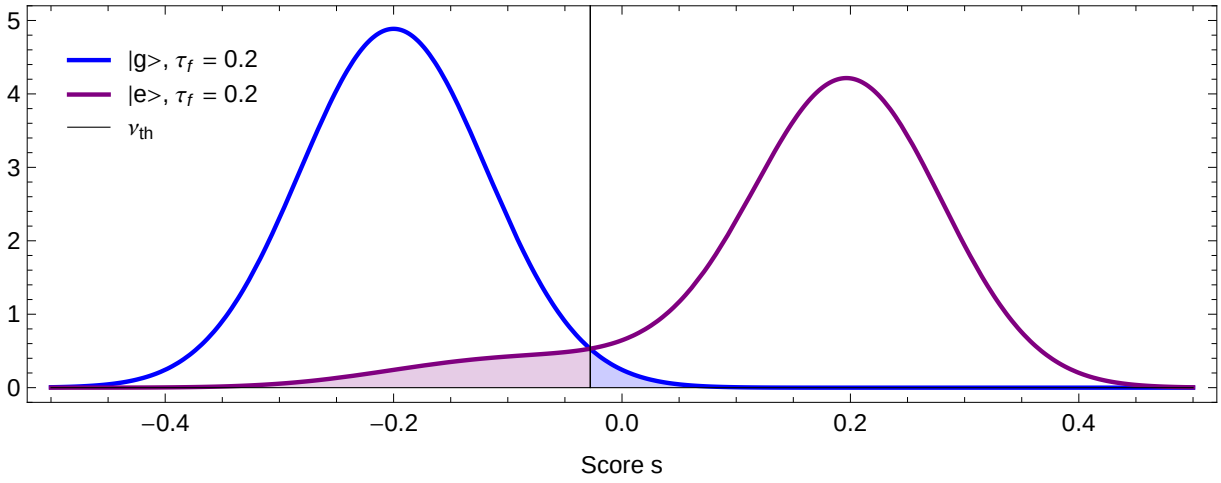


Figure 7.3: Probability distributions for score s with the qubit initially in state $|g\rangle$ or $|e\rangle$ for $\tau_f = 0.2$ at a integrated signal to noise ratio $r_{\mathrm{sn}} = 30$. The read out fidelity F is defined as one minus the shaded area. Every movement of the threshold value ν_{th} results in a reduced fidelity as one area gets smaller but the other increases faster.

probability distributions the fidelity is zero. Different ordering of the two distributions (the excited state distribution $P_{|e\rangle}(s)$ left to the ground state distribution $P_{|g\rangle}(s)$, which is always possible in the experiment, for example when the phase of the I-Q-plane is π) the fidelity is negative with a minimum of -1 for completely separated distributions. A fidelity of -1 is comparable to a fidelity of 1 because more states are falsely classified, so that the assignment needs just to be reversed to identify more states correctly. The integration Equation (7.5) can be computed in closed form (Gambetta et al., 2007) using the probability distributions for the box car integration scores (Equation (7.2) and (7.4)) as

$$F = \tfrac{1}{2}\, e^{\sigma^2/8-(\nu_{\mathrm{th}}+\tau)/2} \left[\mathrm{erf}\left(\frac{\sigma^2-2(\nu_{\mathrm{th}}-\tau)}{2\sqrt{2}\,\sigma}\right) - \mathrm{erf}\left(\frac{\sigma^2-2(\nu_{\mathrm{th}}+\tau)}{2\sqrt{2}\,\sigma}\right)\right]. \tag{7.6}$$

Another way to visualise the fidelity is shown in Figure 7.4. The cumulative score distribution functions corresponding to $P_{|g\rangle}(s)$ and $P_{|e\rangle}(s)$ are calculated and the difference between them (length of the $\nu_{\mathrm{th,opt}}$-line) corresponds to the definition of the fidelity (Equation (7.5)).

7.2.2 Optimisation

As described in Section 7.2.1 the fidelity is maximised with respect to ν_{th} at the intersection point of the two probability distributions

$$P_{|e\rangle}(\nu_{\mathrm{th,opt}}) = P_{|g\rangle}(\nu_{\mathrm{th,opt}}).$$

Unfortunately, this is not solvable for $\nu_{\mathrm{th,opt}}$ in closed form. For every desired integration time τ_f and integrated signal to noise ratio r_{sn} which is hidden in σ a numerical approxi-

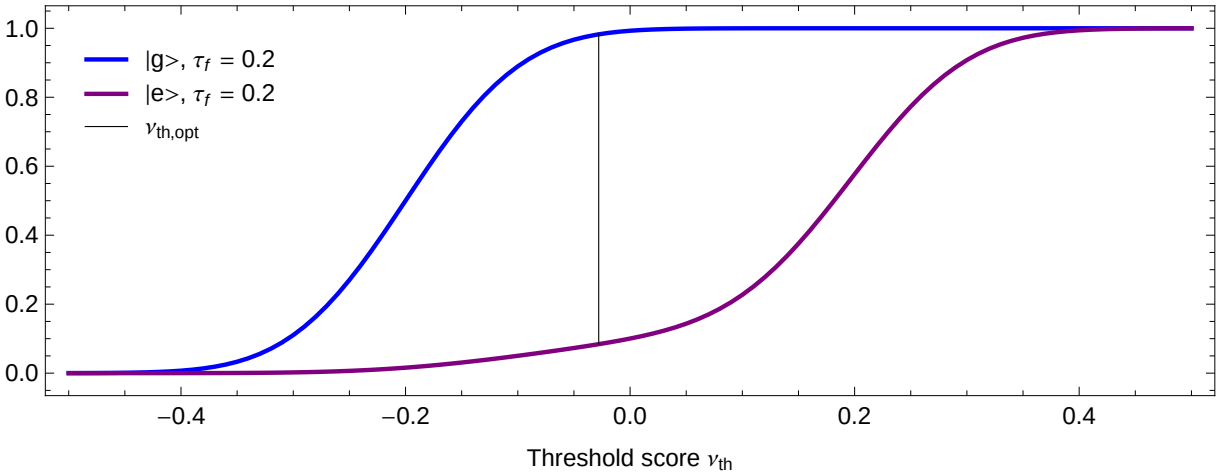


Figure 7.4: "S-curves": cumulative score distribution functions at $r_{sn} = 30$ for $\tau_f = 0.2$. The blue curve corresponds to the sum of the first and third summand in Equation (7.5). The purple curve is the negative of the second summand in Equation (7.5). The length of the black line is therefore exactly the fidelity here shown at its optimal threshold $\nu_{th,opt}$.

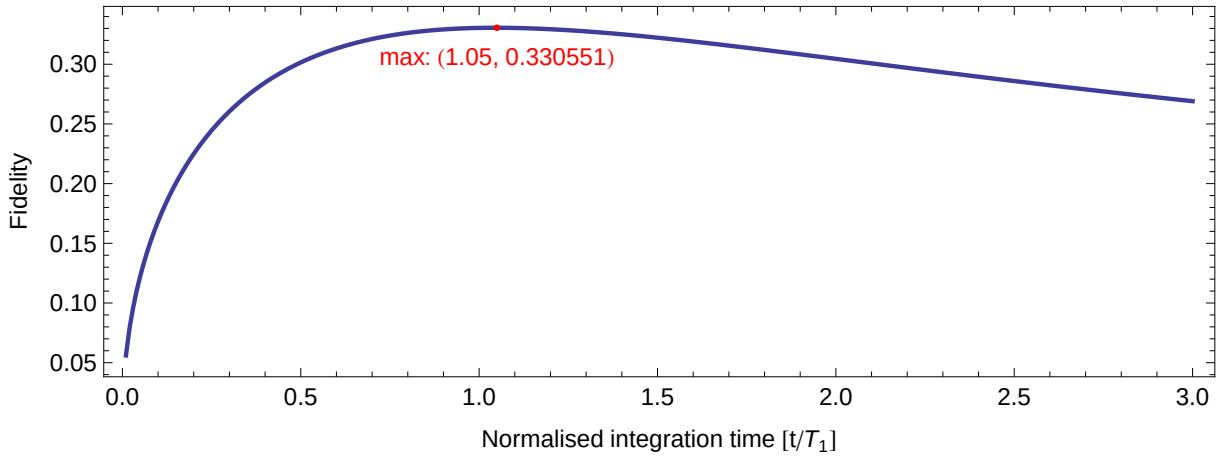


Figure 7.5: Fidelity F using the optimal threshold score $\nu_{th,opt}(\tau_f, r_{sn})$ at integration time τ_f. The integrated signal to noise ratio is fixed at $r_{sn} = 0.5$. F is maximised at a non trivial time $\tau_f = 1.05$ resulting in $F \approx 33\,\%$. A longer or shorter integration time τ_f decreases F.

mation needs to be calculated, as $\nu_{th,opt}$ depends on the two parameters: $\nu_{th,opt}(\tau_f, r_{sn})$.

Once the optimal threshold is found the integration time $\tau_f(r_{sn})$ can be optimised inserting $\nu_{th,opt}(\tau_f, r_{sn})$ in Equation (7.6) and calculating the resulting fidelity, compare Figure 7.5. Searching for the maximal fidelity with respect to τ_f shows that there exists an optimal integration time $\tau_{f,opt}(r_{sn})$. The optimal threshold $\nu_{th,opt}(\tau_{f,opt}(r_{sn}), r_{sn})$ and the optimal integration time $\tau_{f,opt}(r_{sn})$ can be calculated in dependence of r_{sn}, compare Figure 7.6. The higher the signal to noise ratio the faster the measurement completes (Gambetta et al., 2007).

For the optimal parameter $\nu_{th,opt}$ and $\tau_{f,opt}$ the maximally reachable fidelity $F_{opt}(r_{sn})$ can

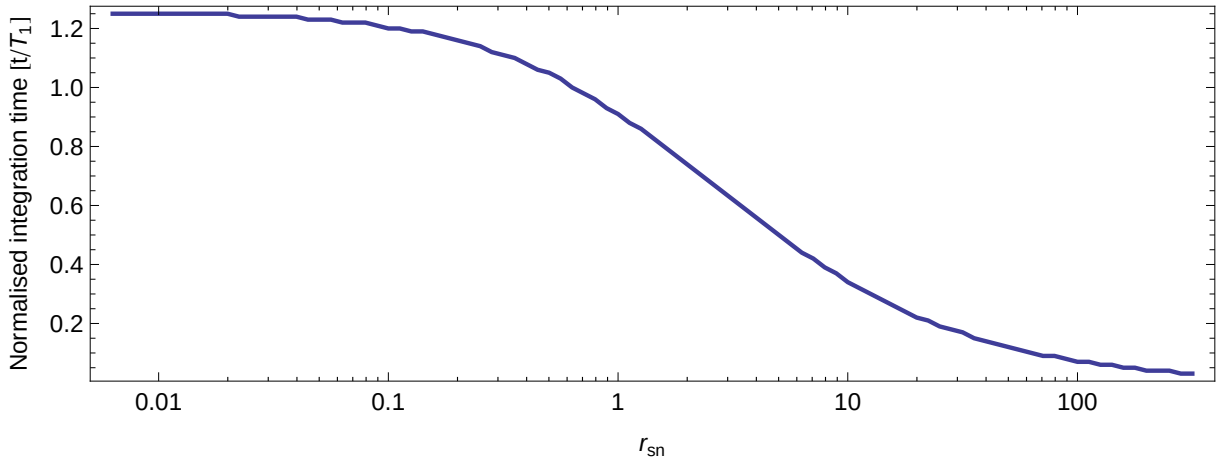


Figure 7.6: Optimal integration time $\tau_{f,\mathrm{opt}}(r_{\mathrm{sn}})$ against integrated signal to noise ratio r_{sn}. Higher r_{sn} complete the measurement faster than low r_{sn}.

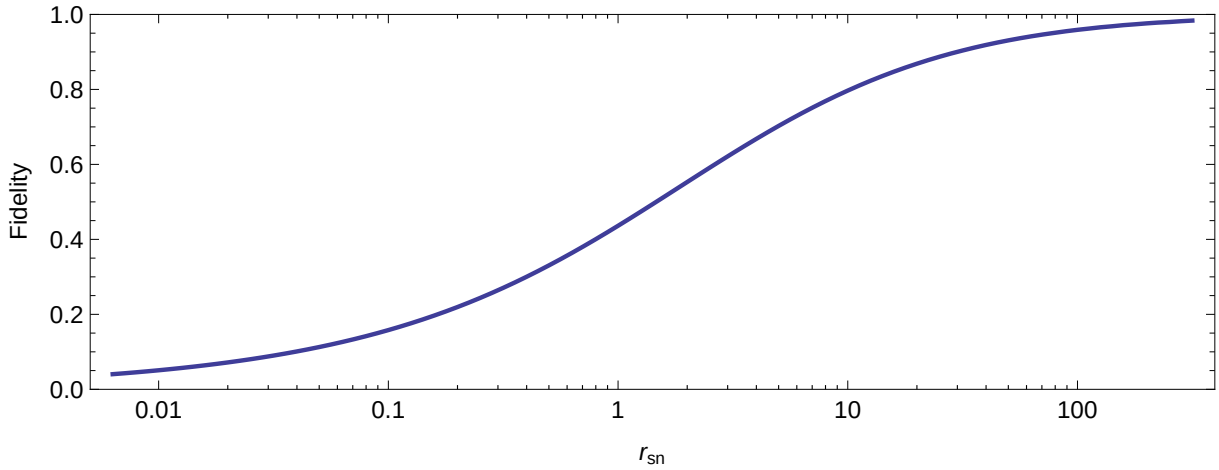


Figure 7.7: Maximal reachable fidelity $F_{\mathrm{opt}}(r_{\mathrm{sn}})$ at integrated signal to noise ratio r_{sn}. Doubling or halving r_{sn} in the region of $r_{\mathrm{sn}} \approx 1$ results in 10 % higher or lower F respectively.

be calculated, compare Figure 7.7. As expected $F_{\mathrm{opt}}(r_{\mathrm{sn}})$ increases for larger r_{sn} and converges slowly to one. Increasing the fidelity when already close to one is more difficult the higher r_{sn} is.

7.2.3 Experimental calculation

To apply the fidelity calculation described above on experimental data some adjustments are necessary. For initial qubit state $|g\rangle$ and $|e\rangle$ the histograms of the probability densities for experimentally measured scores $s_{j,|g\rangle}$ and $s_{j,|e\rangle}$ (living in the complex I-Q-plane) are shown in Figure 7.8. The histograms are the discrete version of the continuous probability distributions $P_{|e\rangle}(s)$ and $P_{|e\rangle}(s)$ with complex scores. The histograms for $P_{|e\rangle}(s)$ and $P_{|e\rangle}(s)$ can be drawn because of good qubit control and accurate preparation of $|g\rangle$ and $|e\rangle$, so

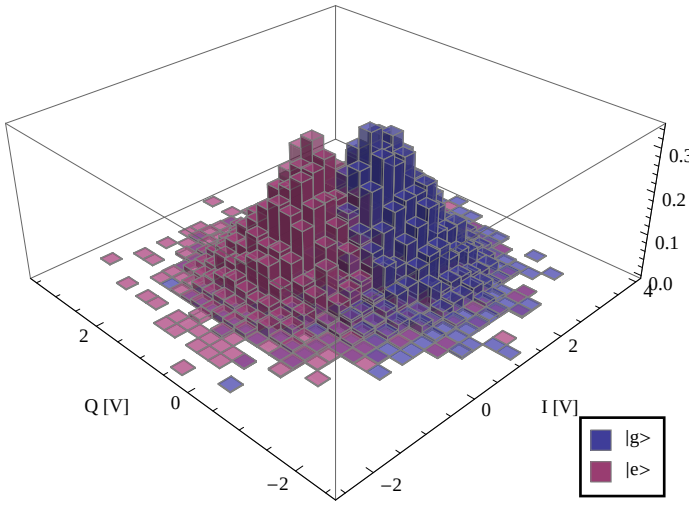


Figure 7.8: Normalised histograms to display probability density $P_{|e\rangle}(s)$ and $P_{|e\rangle}(s)$ of experimentally measured scores $s_{j,|g\rangle}$ and $s_{j,|e\rangle}$. These data are used to find the best criterion for the best assignment to the scores s_j so that the highest fidelity can be achieved.

that we know the state in which the qubit was in the beginning of the measurement when prepared shortly before the measurement. For these complex scores s_j we search for an assignment rule. Corresponding to the threshold score ν_{th} we search for an optimal fidelity with respect to a threshold line. Equivalent to searching a threshold line is to rotate the scores s_j in the I-Q-plane about the origin by an angle φ to $s'_j = \text{rot}_\varphi(s_j) = s_j\, e^{i\varphi}$ and then to optimise a threshold score ν_{th} on the real part of the scores $\Re(s_j\, e^{i\varphi})$. The procedure consists of rotating the scores and then looking on their real part value. This is equivalent to inspecting the one dimensional histograms. For each rotation angle the fidelity is computed for several ν_{th}. The fidelity is calculated using Equation (7.5) but the integrations are represented by discrete sums and $P_{|x\rangle}(s)$ are the histogram bin heights normalised to probabilities with the bin edges are equal to the desired thresholds to be tested. Figure 7.9 shows the "S-curves" on the real part of the rotated scores. The difference between the two "S-curves" is strongly connected to the fidelity (compare Figure 7.4) as here the fidelity at the rotation angel φ and threshold ν_{th} is computed. This difference is shown in Figure 7.10 for the same rotation angle as in Figure 7.9. Repeating this procedure for various rotation angles φ we end up with the fidelities at φ and ν_{th}, compare Figure 7.11. The discontinuity in the centre is related to plotting the absolute fidelity. Due to the rotation the excited state probability distribution $P_{|e\rangle}(s)$ shifts from the right to the left in the real part of the I-Q-plane leading to a negative fidelity (which is as good as a positive one, see Section 7.2.1).

To speed up the calculation only rotation angles φ around the angle between the mean of $P_{|g\rangle}(s)$ and the mean of $P_{|e\rangle}(s)$ are analysed. The range of tested threshold scores are limited as well to be between and a little outside of the two means. After this analysis we end up with the experimental observed read out fidelity F for the experiment with an integration time of t_N, including the optimal threshold line (φ_{opt} and $\nu_{\text{th,opt}}$). A

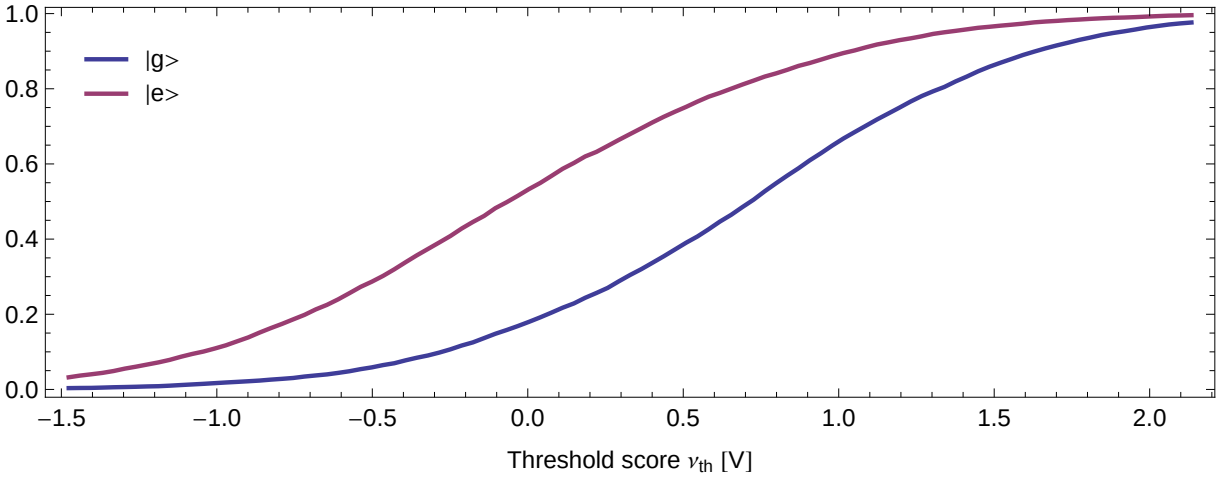


Figure 7.9: "S-curves" of the real part of experimental data after a previous applied rotation with a specific angle (here the optimal angle to achieve the highest fidelity) about the origin.

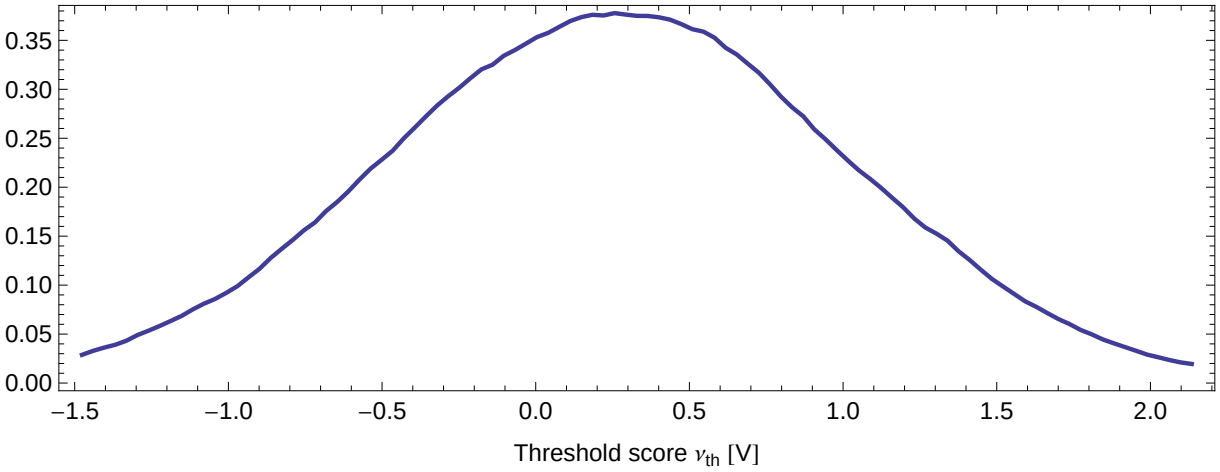


Figure 7.10: Fidelity extracted of the "S-curves" in Figure 7.9 at the optimal rotation angle φ.

two-dimensional histogram for the rotated complex scores displays the largest amount of information. From now on the optimal threshold $\nu_{\mathrm{th,opt}}$ is known which can be used in future measurements to measure an unknown qubit state. The result is shown in Figure 7.12.

If the fidelity is calculated for more than the two different states $|g\rangle$ and $|e\rangle$ the fidelity is calculated for each pair of states. However, only the two outer-most means of the distributions are considered to determine the angles and thresholds to be analysed.

To further improve the read out fidelity a non linear threshold in the complex I-Q-plane was tried out. A polynomial threshold line was thereby used to calculate the fidelity. Points were placed in a graphical I-Q-plane showing the observed score density. The fidelity was calculated using the polynomial threshold line that interpolates the placed points. However, the fidelity was improved only marginally by about 0.1 % not justifying

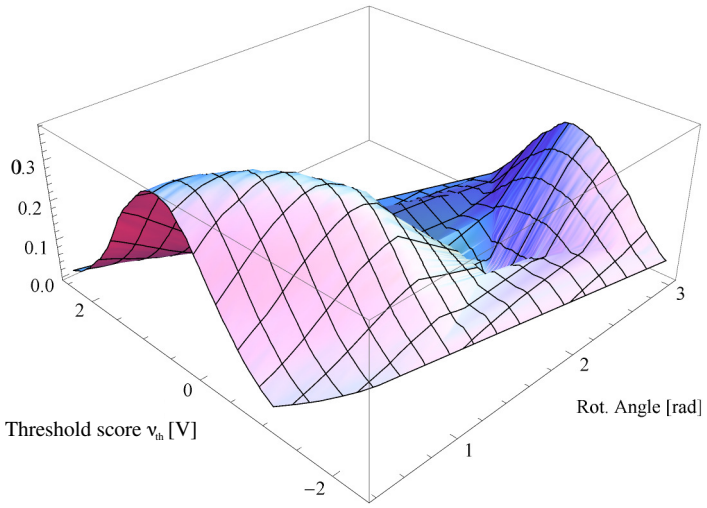


Figure 7.11: Absolute fidelity at different rotation angles φ and different threshold scores ν_{th}. This is the 3D version of Figure 7.10 including many different rotation angles.

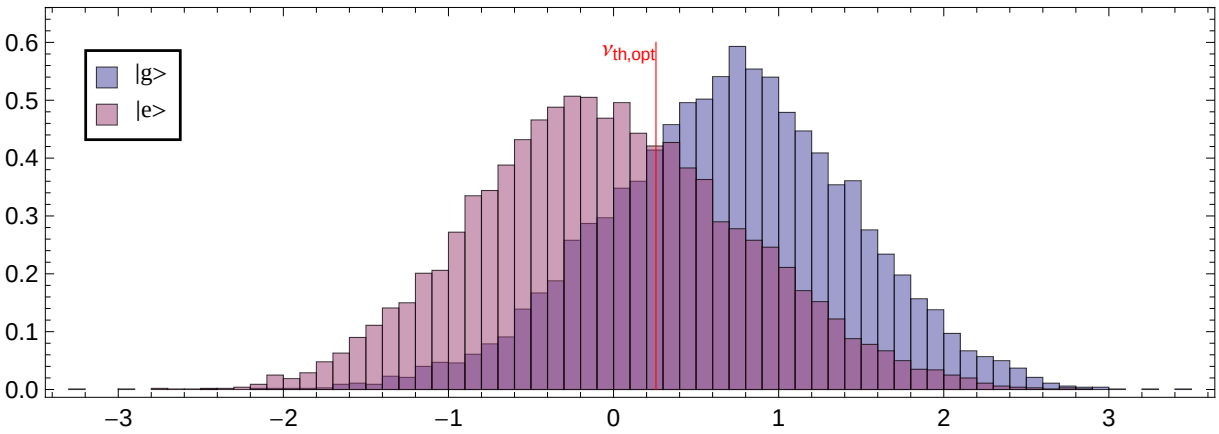


Figure 7.12: Histogram normalised to probability density of the scores $\Re(s_j\, e^{i\varphi_{\mathrm{opt}}})$ (rotated by the optimal angle φ_{opt} and then projected onto the desired quadrature). A fidelity of 37.8 % is reached when choosing the optimal threshold score $\nu_{\mathrm{th,opt}}$ (depicted line).

the complicated threshold line, so that in the following the simpler linear threshold line is used to optimise the fidelity.

7.3 Measurements

The box car integration theory is compared with the experimental result with respect to the integration time t_N and for different integrated signal to noise ratios r_{sn}. For this purpose the mixer in front of the gate line to qubit A is calibrated for the qubit transition frequency $\nu_a \approx 4.47\,\mathrm{GHz}$, see Figure 3.3 for the measurement setup. The sample introduced in Section 3.1 for this comparison that was in our Oxford cryostat was produced

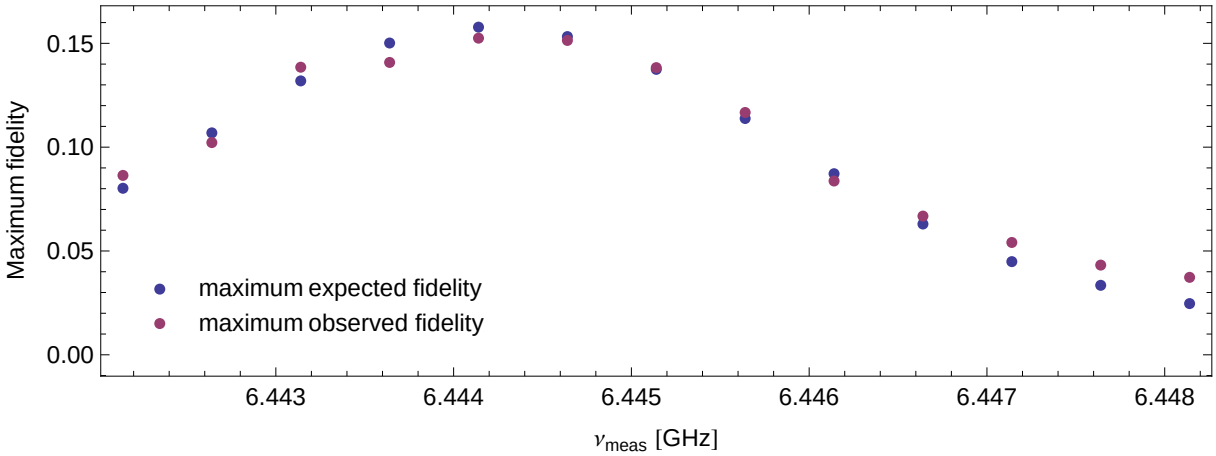


Figure 7.13: Maximal (with respect to the box car integration time) fidelity for different measurement frequencies ν_{meas}. The maximum expected fidelity is calculated based on different r_{sn} for the ν_{meas}. The maximum observed fidelity is the experimentally maximal observed fidelity with respect to the integration time t_N.

by Göppl (2009). A π-pulse on qubit A through the gate line was calibrated with a Rabi experiment followed by a pulsed resonator transmission measurement. The following measurements were done in parallel on the one hand with the averager of the long established AQC and on the other hand with the SSSv3 application running on the FPGA card using different integration lengths t_N. The intermediate frequency was chosen to $\nu_{\text{if}} = 25\,\text{MHz}$ to have a better time resolution of $1/\nu_{\text{if}} = 40\,\text{ns}$. The qubit state was then measured with different measurement frequencies ν_{meas} and different measurement powers $\langle n \rangle$ (average measurement photon number, in the case of measuring at the resonators resonance frequency). This procedure is performed for the qubit prepared in the excited state $|e\rangle$ (applying a π-pulse exactly before the pulsed measurement) and for the qubit prepared in the ground state $|g\rangle$ (no π-pulse). We received a set of averaged measurement responses for different ν_{meas} and $\langle n \rangle$ which could then be analysed with the cavity Bloch equations (compare Section 3.3). Additionally we got the same set of measurement responses in the form of single shot integrated scores $s_{j,|x\rangle}$, $j = 1, \ldots, 10\,000$ for different integration times t_N.

To fit the measurement response with the different measurement frequencies ν_{meas} a cavity Bloch fit was performed. At measurement powers higher than -19 dBm ($\langle n \rangle \approx 9$) the theoretical considerations in the cavity Bloch equations seem to break down, so we choose the measurement power of $\langle n \rangle \approx 9$ for further analyses. Nevertheless different integrated signal to noise ratios r_{sn} will be received for the comparison with the predicted single shot read out fidelity as different ν_{meas} were used for fitting reasons to the cavity Bloch equations. After fitting the cavity Bloch equations to the measured averaged data the signal to noise ratios r_{sn} integrated over time $T_1 = 520\,\text{ns}$ could be calculated for different ν_{meas} as it was done in Section 6.5. Figure 6.11 shows the obtained r_{sn} for this measurement. As in Section 7.2.2 we could calculate the maximal attainable fidelity for the different r_{sn} which is shown in Figure 7.13

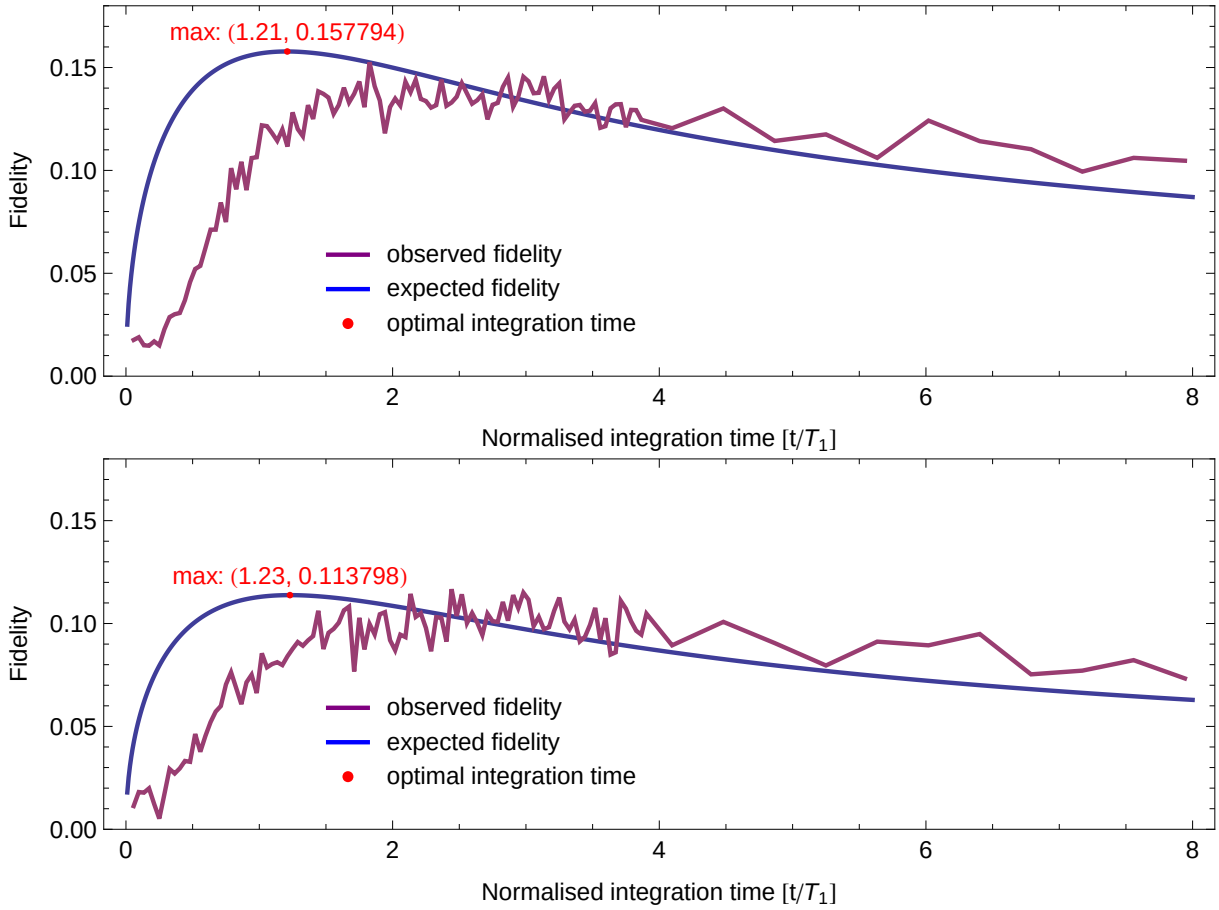


Figure 7.14: Behaviour of observed and theoretical fidelity for different integration times τ_f at two different measurement frequencies $\nu_{\text{meas}} = 6.44414\,\text{GHz}$ (top, $r_{\text{sn}} \approx 0.10$) and $\nu_{\text{meas}} = 6.44564\,\text{GHz}$ (bottom, $r_{\text{sn}} \approx 0.05$).

As explained in Section 7.2.3 the maximal fidelity of the sets of single shot data are extracted for all integration times t_N and measurement frequencies ν_{meas}. The maximum fidelity with respect to t_N for each ν_{meas} is compared with the maximum expected one shown in Figure 7.13. They match very well and have a similar form. In Figure 7.14 the behaviour of the fidelity for the integration time $\tau_f = {}^{t_N}/_{T_1}$ is shown for two different measurement frequencies ν_{meas}. As can be seen the maximal fidelity is reached much later than expected. This can be explained by the fact, that there is no cavity raise time assumed in the single shot box car measurement protocol (see Section 7.1). Nevertheless the height and the form of the expected and observed fidelities are comparable, see Figure 7.14.

To fortify, that disregarding the cavity raise time is the reason for the later observed maximal fidelity, the same experiment was repeated using a new sample with a much faster cavity raise time. This sample with one transmon placed in a lower Q (inverse proportional to κ) resonator was produced by Johannes Fink and mounted in our "Vericold" cryostat. The main parameter change of our interest is the photon decay rate κ. In the previous experiment it was ${}^{\kappa}/_{2\pi} \approx 1.7\,\text{MHz}$ while using the new sample it is ${}^{\kappa}/_{2\pi} \approx 11\,\text{MHz}$ which

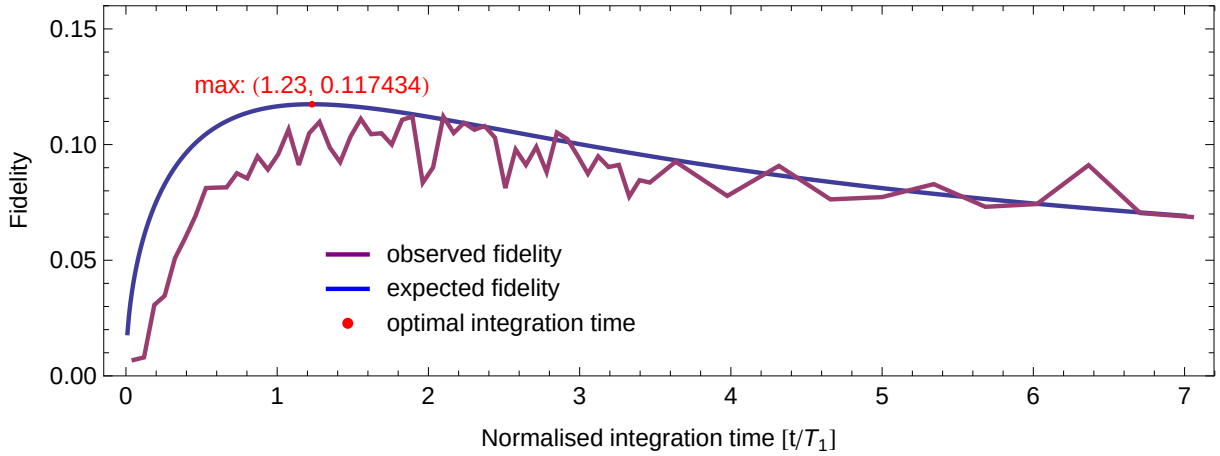


Figure 7.15: Behaviour of observed and theoretical fidelity for different integration times τ_f measured at $\nu_{meas} = 6.55583\,\text{GHz}$ ($r_{sn} \approx 0.05$). A faster increasing observed fidelity than in Figure 7.14 is visible as the sample had a higher photon decay rate $\kappa/2\pi \approx 11\,\text{MHz}$ and it fits better to the theoretical expected fidelity.

leads to the faster cavity raise time. The other parameters of the sample were $\nu_{res} \approx 6.55\,\text{GHz}$, $g/2\pi \approx 94\,\text{MHz}$ and the qubit transition frequency was tuned to $\nu_a \approx 5.3\,\text{GHz}$ during the measurement. The π-pulse was calibrated and applied directly through the resonator using the modulator of the microwave generator. The averaged data is fitted to the cavity Bloch equations but unfortunately deviations even at low measurement powers existed. Nevertheless a measurement power of $\langle n \rangle \approx 8$ was chosen because at even lower measurement power the experimental observed fidelities were very low and their form difficult to analyse. Even the theoretical calculation reached first numerical limits for this case. The fits to the cavity Bloch equations have shown an increasing T_1 with the measurement power indicating some back and forth jumping between $|g\rangle$ and $|e\rangle$ or rather between some entangled states with the cavity, predicted by the dressed dephasing model (Boissonneault et al., 2008). Also other unexplained facts or nonlinearities could have caused the deviations in the cavity Bloch equations showing up in the increasing qubit life time. The integrated signal powers, extracted as in Section 6.5 described, resulted in too high r_{sn} to fit the experimentally observed fidelities. So the integrated signal power, used to calculate r_{sn}, was calculated not from the decay-free qubit but from the averaged measurement response with the decaying qubit. For this r_{sn} the observed fidelity evolution fits better to the expected one, compare Figure 7.15. As can be seen the observed fidelity increases much faster for the high κ sample than for the low κ sample. This fortifies the consideration of cavity raise times in single shot measurement protocols. Another idea to consider is the resonator ringing when measuring the cavity off resonant. However, the integrated powers resulting from this ringing are much smaller than the integrated power in the DC bin of the signal power spectrum.

7.4 Higher qubit states

A single shot analysis with higher qubit states than $|g\rangle$ and $|e\rangle$ was performed. We calibrated a π-pulse from state $|g\rangle$ to $|e\rangle$ equally as the first π-pulse calibration in Section 7.3 with the difference that not the pulse length was varied but the amplitude of a 10 ns pulse. The π-pulse was applied through the gate line to qubit A, compare Figure 3.3 for the experimental setup. A second π-pulse from state $|e\rangle$ to $|f\rangle$ is calibrated varying the amplitude of another pulse of length 10 ns succeeding directly the first π-pulse (from state $|g\rangle$ to $|e\rangle$) with a second generator. This generator guides passing a mixer and an amplifier (see Figure 3.3) into the gate line to qubit A. Of course, beforehand the mixer used was calibrated at the frequencies needed. Shortly before the measurement starts the $|f\rangle$ state can now be prepared by applying the two π-pulses successively. The three pulse series are joined leading to a sequence of qubit states in the order $|g\rangle$, $|e\rangle$ and $|f\rangle$.

The measurement is done with a measurement frequency $\nu_{\text{meas}} = \nu_{\text{res},|g\rangle}$, where $\nu_{\text{res},|g\rangle}$ is the resonance frequency of the sample measured with qubit state $|g\rangle$, at different powers and IF $\nu_{\text{if}} = 25\,\text{MHz}$. The measurement response was then analysed with the FPGA card using the SSSv3 single shot box car integration for different integration times. After integrating $t_N = 590\,\text{ns}$ the maximal read out fidelity (discriminating $|g\rangle$ and an excited state $|e\rangle$ or $|f\rangle$) was achieved for both excited states at the same measurement power. Here we achieved about 10 % better fidelity for discriminating between $|g\rangle$ and $|f\rangle$ than between $|g\rangle$ and $|e\rangle$ as shown in Figure 7.16. The higher fidelity results from a larger signal to noise ratio because the $|f\rangle$ state shifts the resonator further away from $|g\rangle$ as the $|e\rangle$ state does leading to a better contrast in the transmission in comparison to the $|g\rangle$ state transmission.

This could be a scheme to improve the read-out fidelity. Just a π-pulse is applied from $|e\rangle$ to $|f\rangle$ (or even higher states) exactly before the measurement pulse to increase the single shot signal to noise ratio leading to a better read out fidelity.

7.5 Multi-qubit read-out

A single shot analysis with a joined read out of two qubits in a single resonator was performed. The qubits were driven independently through their gate lines with the "Spec" generators guiding directly into the qubit gate line passing only a mixer, compare Figure 3.3. Qubit A was tuned to 5.04 GHz and qubit B to 4.46 GHz for which similar decay times $T_1 \approx 0.5\,\mu\text{s}$ are expected and the steady state resonators for $|ee\rangle$, $|eg\rangle$, $|ge\rangle$, $|gg\rangle$ are approximately equidistantly distributed. For both qubits π-pulses of length 10 ns were calibrated so that the qubits can be individually excited from state $|g\rangle$ to $|e\rangle$. Then we performed a single shot analysis on the sequence $|gg\rangle$, $|eg\rangle$, $|ge\rangle$, $|ee\rangle$ where the last state was generated for both qubits simultaneously. At an example measurement frequency of $\nu_{\text{meas}} = 6.4527\,\text{GHz}$ (intended to be between $\nu_{|gg\rangle}$ and $\nu_{|ge\rangle}$) the maximal fidelity discriminating state $|gg\rangle$ and $|ee\rangle$ was achieved with integration time $t_N = 950\,\text{ns}$ and a measurement power of $\langle n\rangle \approx 47$. The histograms for the measurement where this maxi-

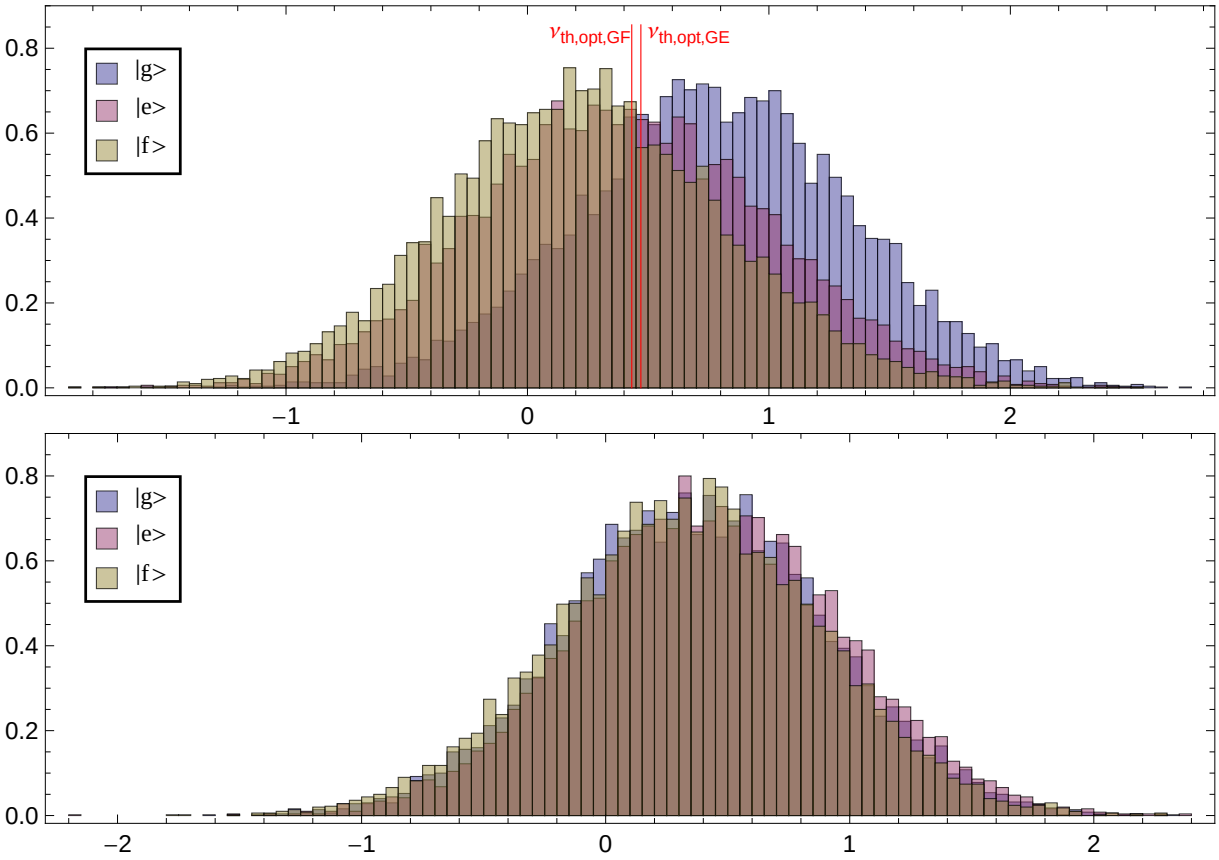


Figure 7.16: Histograms for the single shot scores $s_{j,|x\rangle}$ normalised to the probability density of the initial qubit state $|g\rangle$, $|e\rangle$ and $|f\rangle$ respectively. The read out fidelity reached is $F_{|g\rangle,|e\rangle} = 27\%$ and $F_{|g\rangle,|f\rangle} = 38\%$ with thresholds (vertical lines) drawn to discriminate. Top: Scores rotated in the I-Q-plane by φ_{opt} to achieve the clearest distribution separation in $\Re(s_{j,|x\rangle}\, e^{i\,\varphi_{\text{opt}}})$. Bottom: Histograms in the orthogonal direction $\Im(s_{j,|x\rangle}\, e^{i\,\varphi_{\text{opt}}})$ indicating that the three distributions are very similar and almost no separation is visible.

mal fidelity was reached are shown in Figure 7.17. In the top figure the single shot data is rotated to achieve the best separation of the $|gg\rangle$ and $|ee\rangle$ distribution. In the other quadrature (bottom histogram in Figure 7.17) the histograms are not well separated indicating that most information is in the first quadrature. The fidelities for discriminating all four different states are given by

$$F = \left(\begin{array}{c|ccc} & |eg\rangle & |ge\rangle & |ee\rangle \\ \hline |gg\rangle & 0.2387 & 0.2769 & 0.3769 \\ |eg\rangle & & 0.0982 & 0.1416 \\ |ge\rangle & & & 0.1465 \end{array}\right).$$

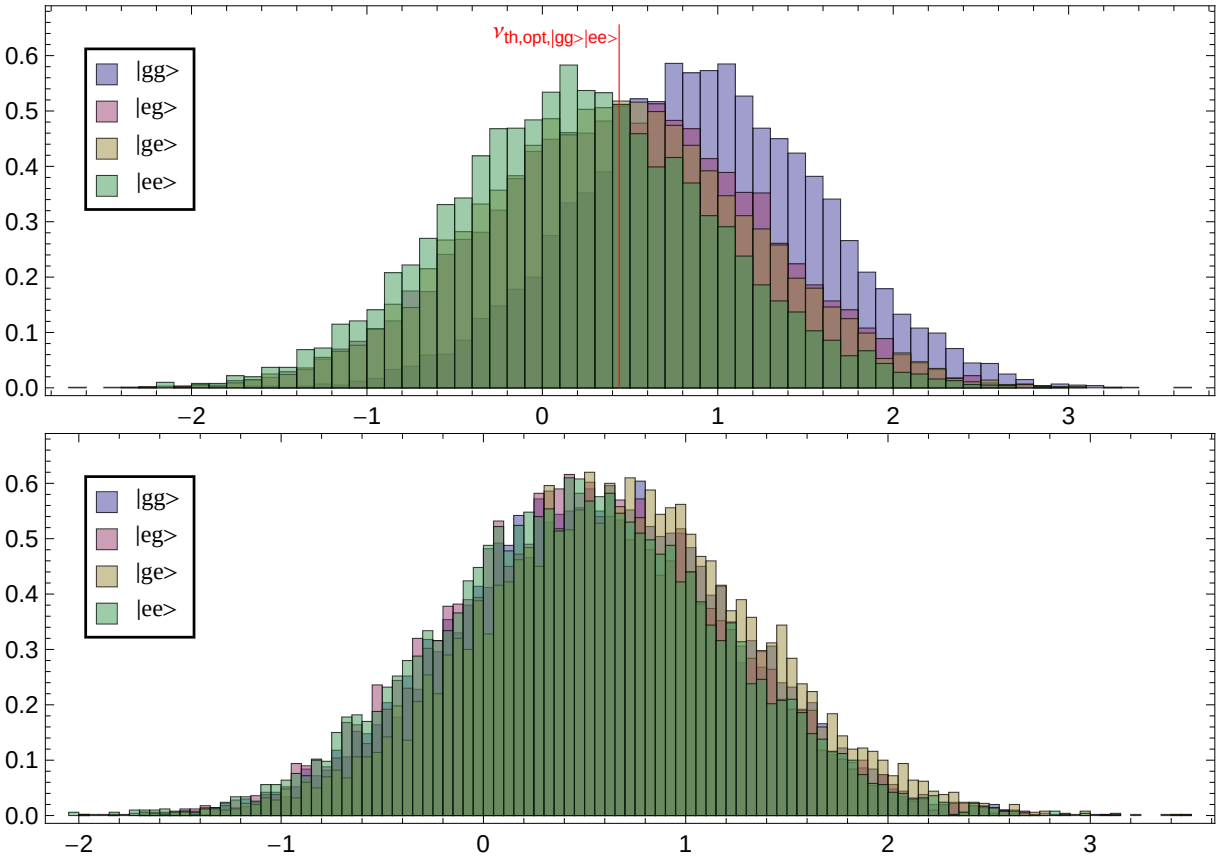


Figure 7.17: Histograms for the single shot scores $s_{j,|xx\rangle}$ normalised to the probability density of the initial qubit state $|gg\rangle$, $|eg\rangle$, $|ge\rangle$ and $|ee\rangle$ respectively. The read out fidelity reached is e.g. $F_{|gg\rangle,|ee\rangle} \approx 38\%$ and $F_{|eg\rangle,|ge\rangle} \approx 10\%$. Top: Scores rotated in the I-Q-plane by φ_{opt} to achieve the clearest distribution separation in $\Re(s_{j,|x\rangle}\, e^{i\,\varphi_{\text{opt}}})$. Bottom: Histograms in the orthogonal direction $\Im(s_{j,|x\rangle}\, e^{i\,\varphi_{\text{opt}}})$ indicating that the three distributions are very similar and almost no separation is visible.

7.6 Bifurcation regime

As far as I know measurements performed at such high measurement powers, as presented in this section, are theoretically not understood yet at an applicable level. Nevertheless I would like show some single shot results because significantly better read out fidelities were reached.

During the measurement of the multi-qubit read out (Section 7.5) a second resonance frequency ν_2, in addition to the normal resonance frequency ($\nu_{\text{res},|gg\rangle}$ with the qubits in the ground state), about 20 MHz below $\nu_{\text{res},|gg\rangle}$ was observed. This resonance frequency ν_2 was much higher than the normal $\nu_{\text{res},|gg\rangle}$ when spectroscopically investigating the resonator at high power. A single shot analysis on the sequence $|gg\rangle$, $|eg\rangle$, $|ge\rangle$, $|ee\rangle$ (compare Section 7.5) was performed with measurement frequency $\nu_{\text{meas}} \approx \nu_2$ and a measurement power of $\langle n\rangle \approx 4500$ (8 dBm). The highest read out fidelity was reached

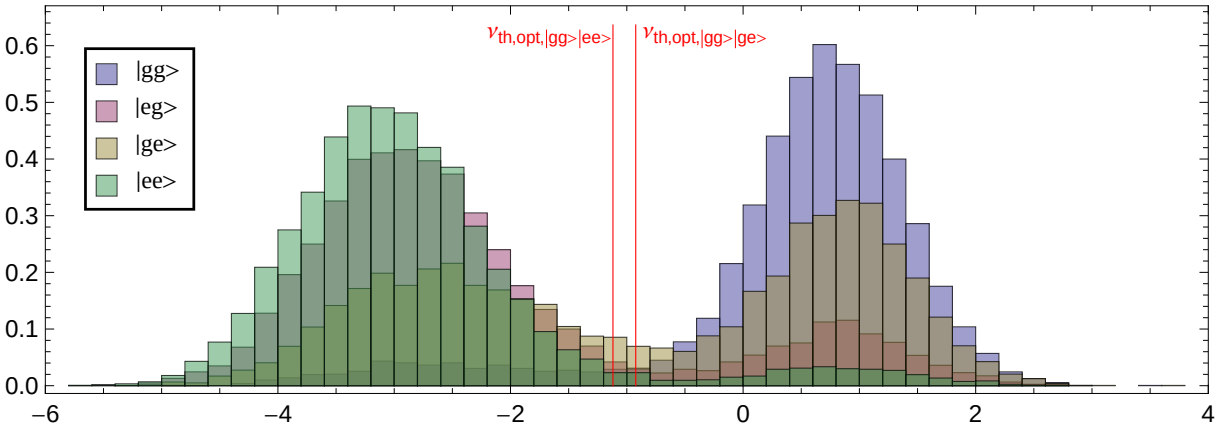


Figure 7.18: Histograms for the single shot scores $s_{j,|xx\rangle}$ normalised to the probability density of the initial qubit state $|gg\rangle$, $|eg\rangle$, $|ge\rangle$ and $|ee\rangle$ respectively. The read out fidelity reached is e.g. $F_{|gg\rangle,|ee\rangle} \approx 84.6\%$ and $F_{|gg\rangle,|eg\rangle} \approx 73.2\%$. Scores are rotated in the I-Q-plane by φ_{opt} to achieve the clearest distribution separation in $\Re(s_{j,|x\rangle}\, e^{i\,\varphi_{\text{opt}}})$.

at an integration time $t_N = 700\,\text{ns}$. The histograms of this measurement are shown in Figure 7.18. It seems that the resonator is bistable with very low decay rates. There are two stable points in the histogram that are populated mainly by the initial qubit state. The fidelities observed are the highest measured within this experimental setup. The read out fidelity for discriminating state $|gg\rangle$ and $|ee\rangle$ is $F_{|gg\rangle,|ee\rangle} = 84.6\,\%$. Even the discrimination of a single qubit reached the best read out fidelity of $F_{|gg\rangle,|eg\rangle} = 73.2\,\%$. Probably the fidelities could be further improved. However, we are mainly interested in investigating low power measurements that are already theoretically understood.

Chapter 8

Summary

The main goal of this thesis was to integrate a single shot read-out for qubit states into the experimental circuit quantum electrodynamics (QED) setup used in our laboratory. A field programmable gate array (FPGA) card comprising external random access memory (RAM), PCI interface and digital input and output was programmed. Furthermore the card offers an external clock input for phase locking of the FPGA to the experiment, digital to analog converters (DACs) for analog output of digital signals and analog to digital converters (ADCs). The latter convert the analog input signal to a time discrete digital signal, which is then further processed on the FPGA in a parallel way. The FPGA was programmed such that its components are controlled by a "wrapper"-block which includes a digital signal processing and analysis block ("user app component"). By graphically designed FPGA code the "user app component" can be easily extended or modified. Modifications do hereby not require any changes in the FPGA control, making the FPGA and its digital signal analysis very flexible. A new C-library, which can be called via LabVIEW, was implemented to control the FPGA and its measurements. The digital "user app component" was programmed to perform real-time digital downconversion of a heterodyne signal, signal recording, basic signal averaging and single shot signal analysis. The FPGA was fully integrated into the experimental setup and can be controlled by the standard software that operates the experiment.

The digital signal processing of the FPGA was analysed theoretically and experimentally resulting in good agreement. The consistency with existing measurement routines as well as the performance of the applications running on the FPGA were verified with the gained expertise. By means of single shot measurements, signal and noise of the experimental setup were analysed. We found an expected noise power of around 60 noise photons caused by the amplifier chain which limits the read-out fidelity.

By integration of the measurement signal, single shot read-out of qubit states was performed. The single shot measurements were analysed and the decision function used for inferring the qubit state was optimised to enhance the qubit read-out fidelity. Furthermore the integration time for the single shot measurement was optimised. At low measurement powers, a comparison of the experimentally observed single shot read-out performance with the theoretically expected one showed good agreement. Here fidelities of around 10 % were reached. For higher measurement powers significantly higher fidelities could be obtained (up to 73 %). Note that a comparison to theoretical expectations was here

not possible, since the high power dynamics is not well explored yet and therefore the parameters did not fit into the single shot measurement theory.

Additionally multi-qubit single shot read-out was demonstrated. Here high power measurements resulted in single shot read-out fidelities of up to 84 % for two qubits and 73 % for a single qubit. Furthermore, a scheme to increase the read-out fidelity was elaborated. For the case in which the qubit is in the excited state it is excited to a higher energy level just before the single shot integration. This leads to a stronger signal and therefore a better accuracy of discrimination.

To conclude, we have entered a novel regime of measurements in making the transition from an averaged ensemble measurement towards single shot measurements. This has been confirmed with a comparison to theoretical expectations for single shot read-out (Gambetta et al., 2007). The real-time single shot read-out allows for new studies and experiments and provides the basis for further extensions, such as measurement feedback on the qubit state as well as error correction algorithms.

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Ich versichere, dass ich diese Diplomarbeit selbständig verfasst und nur die angegebenen Quellen und Hilfsmittel verwendet habe.

9.6.2009 _____

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